Synthelog III

— 82.9 —

Bouwboek MASTER

Synthelog III

— 82.9 ——

verbeterde versie

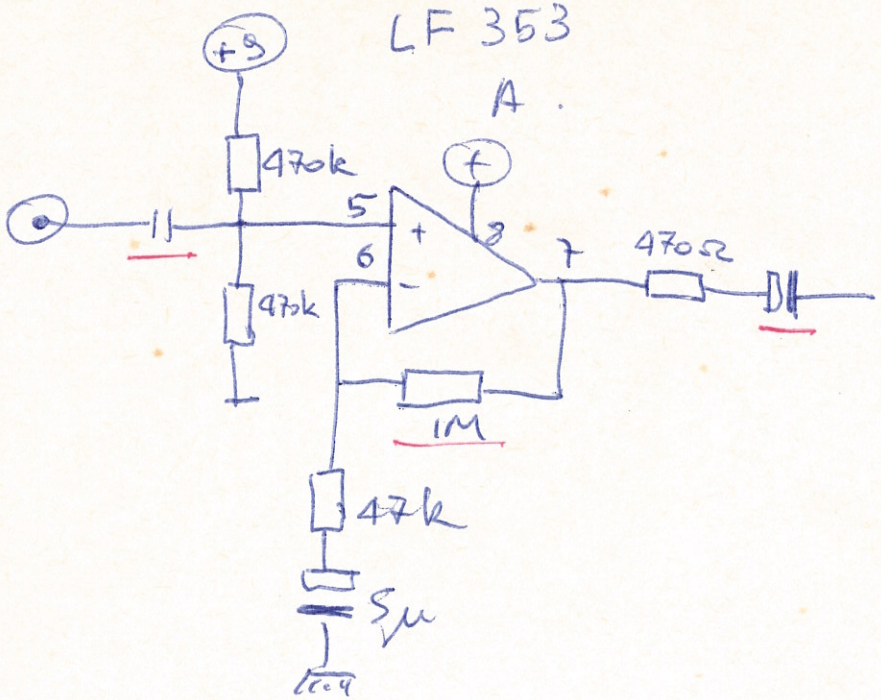
4 exemplaren.

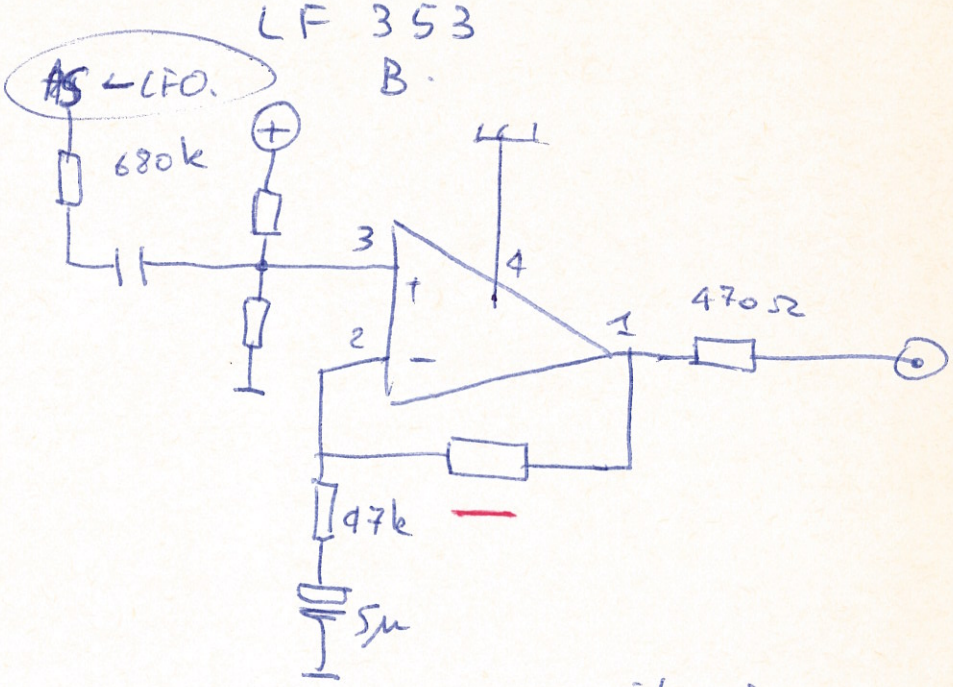
RAES
82.9
3140
HOLD
ATTACK
DECAY
Level
LFO
VCO
FILT.
7493
556
380
LM317
+5
+9

RAES
82.9
3140
LFO
ATTACK
DECAY
Level
VCO
FILT.
7493
556
380
LM317
+5
+9

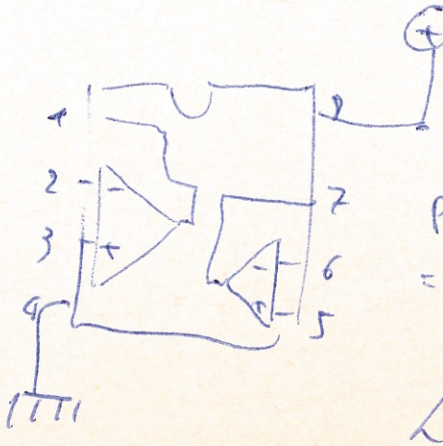
5 4

5 4





— = nog niet op print bestudeerd



pin to pin
= XR 4558
= 2x 741
~~EXR 5532~~
LF 353
pin to pin
= TL082
~~TL083~~
Latch-up free

is er niet bij
- inbouwdoos
- een "x" aantal - schakelaars
- jacks en pluggen
waarvoor enige —□— 1k bijhoren
- transformator

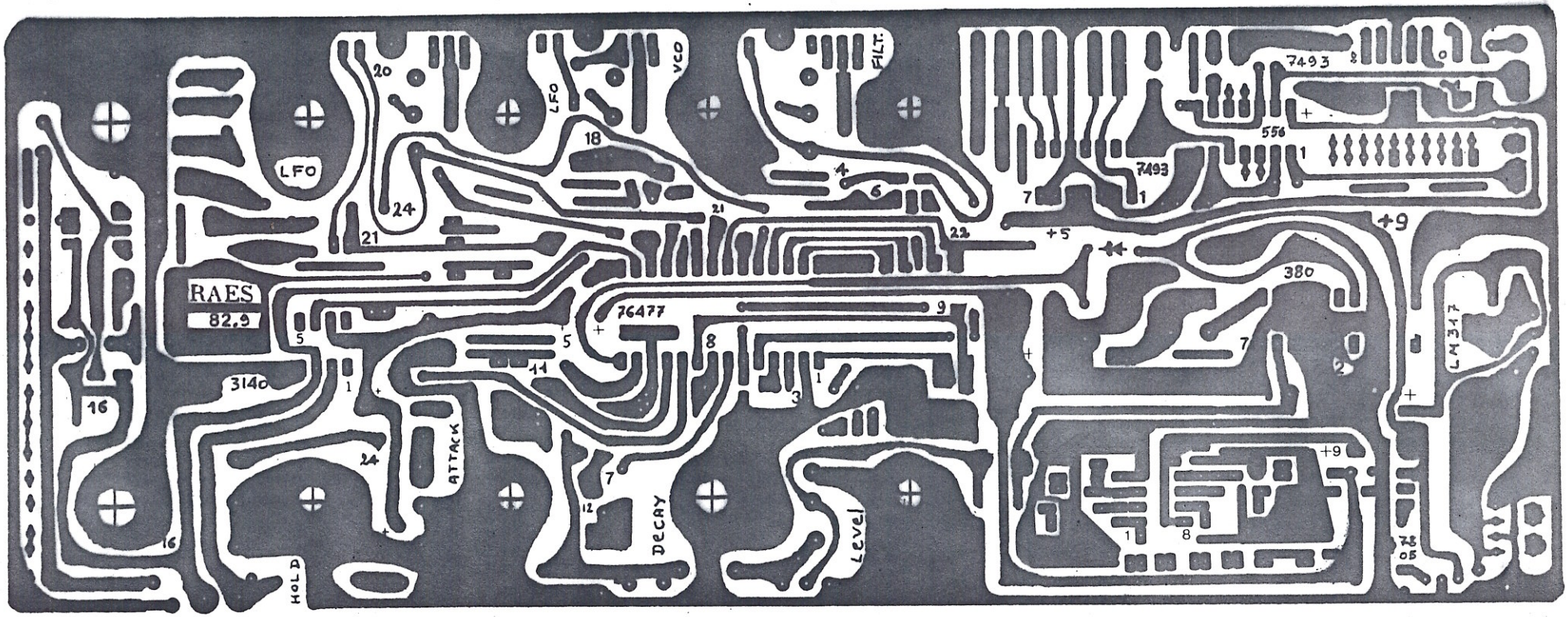
~~wel~~ behoort tot het ~~in~~bouwpakket

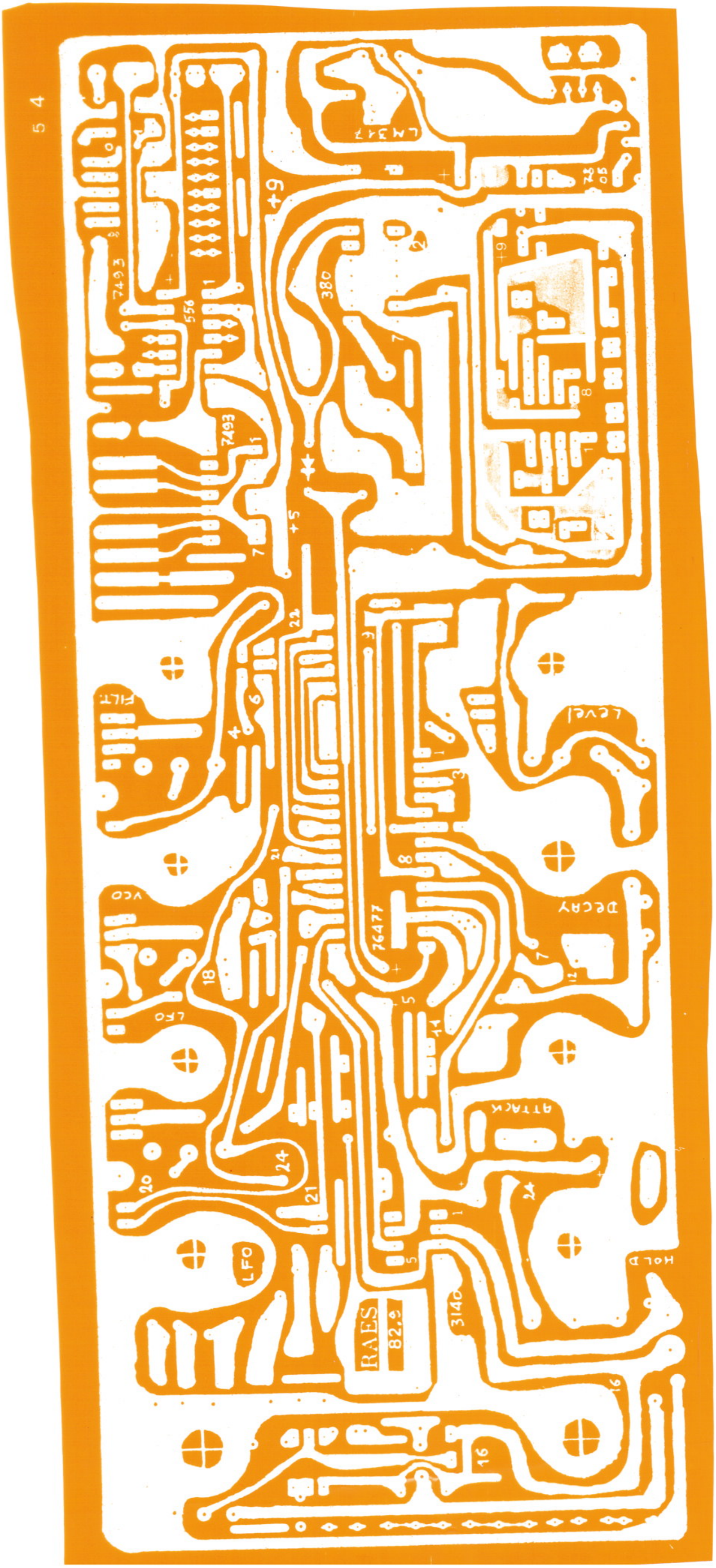
- 1 led
- ◪ bij 470 KB 6X
220 KB 2X
47 2X
1M 4X
- ~~range-pot~~ 2X 6 standen draaischak.
- mini-speakertje 0,1W 8Ω
- IC SN 76477 N
CA 3140
LM 380N
NE 556 N
SN 7493 N
7805 C
LM 317

- dioden 5X BY127
- regelbare —□— 4k7 Trimpot.
- —□— 220 k 2X
47 k 5X
680k 1X
3k3 6X
3k9 1X
4k7 2X
10k 1X
2k7 1X
39k 1X
22k 1X
470 3X
120 1X
1k 2X

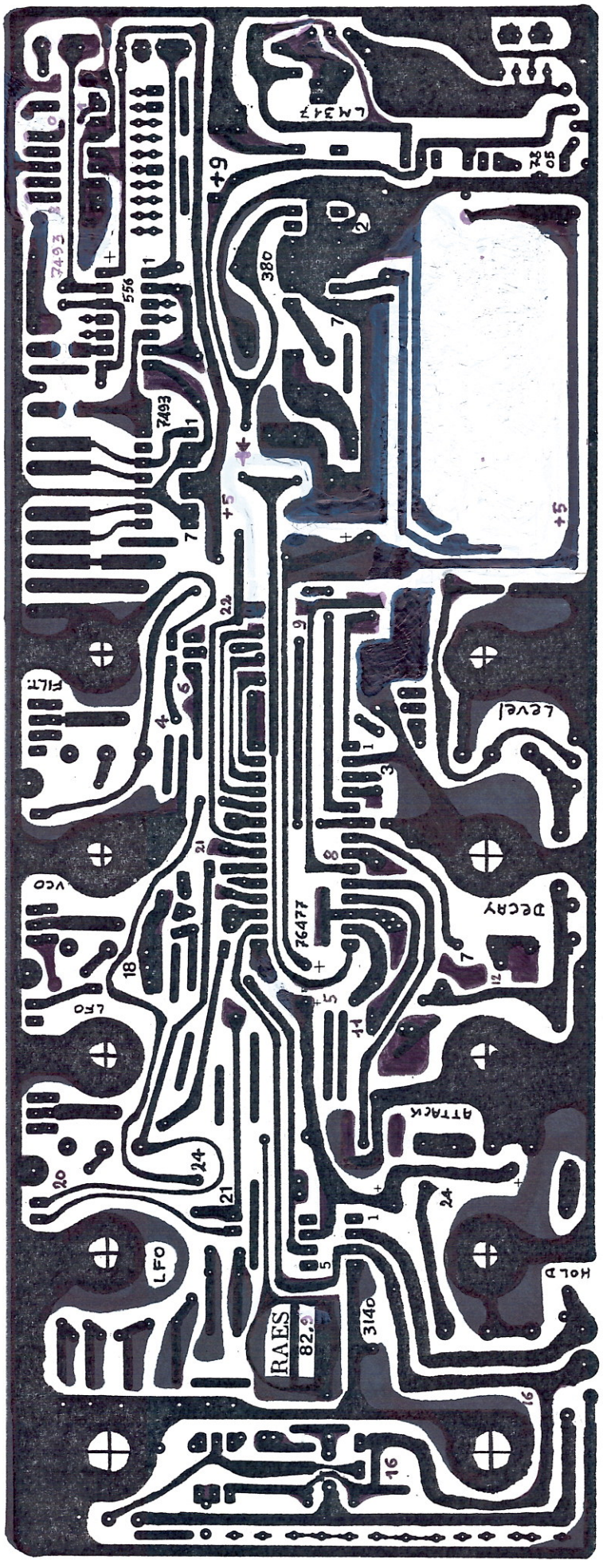
—|— 4700 µ 1X
470 µ 2X
1000 µ 1X
10 µ 3X
1 µ 2X
100 n 4X
10 n 1X
1 n 4X
500 pF 1X
4,7µ 3X
3,3µ 2X
22 n 1X
4n7 1X
0,68µ 1X

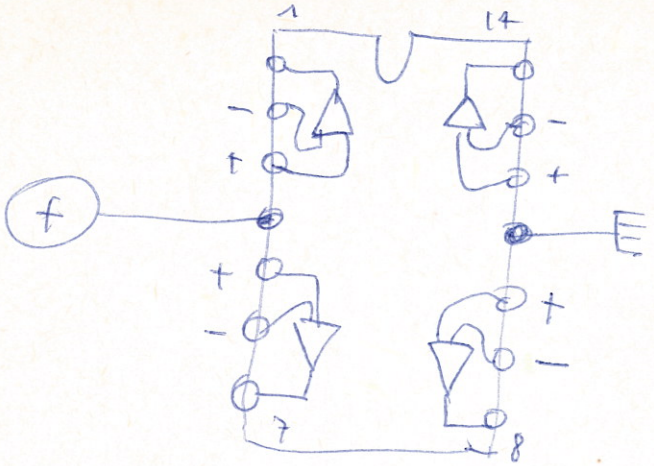
} 12V


RAES
82.9
LFO
LFO
VCO
FILT.
7493
7493
556
3140
76477
ATTACK
DECAY
LEVEL
HOLD
380
LM317
+5
+9

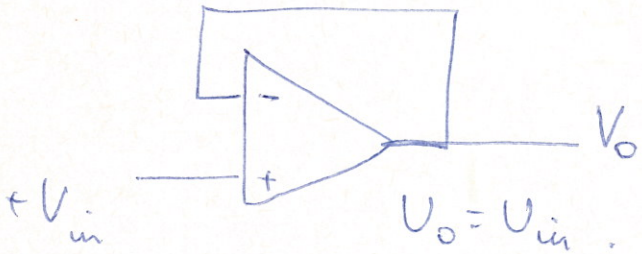


7493
556
+9
380
+5
7493
FILT
VCO
LFO
LEVEL
DECAY
ATTACK
HOLD
76477
3140
RAES
82.9


LM317
2x
gewoon
hand
kontrast
RAES
82.9
FM317
7805
7493
556
380
7493
+9
+5
+5
FILT
LEVEL
VCO
DECAY
76477
LFO
ATTACK
LFO
HOLD
3140

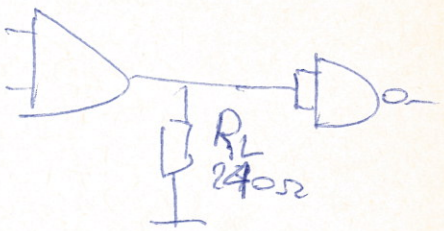


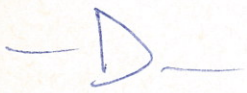
LM124
224
324
124A
224A
324A
LM2902.



$U_o = U_{in}$.

TTL-Driving:

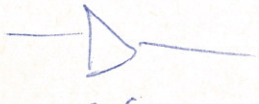




LFO

VCO

Noise



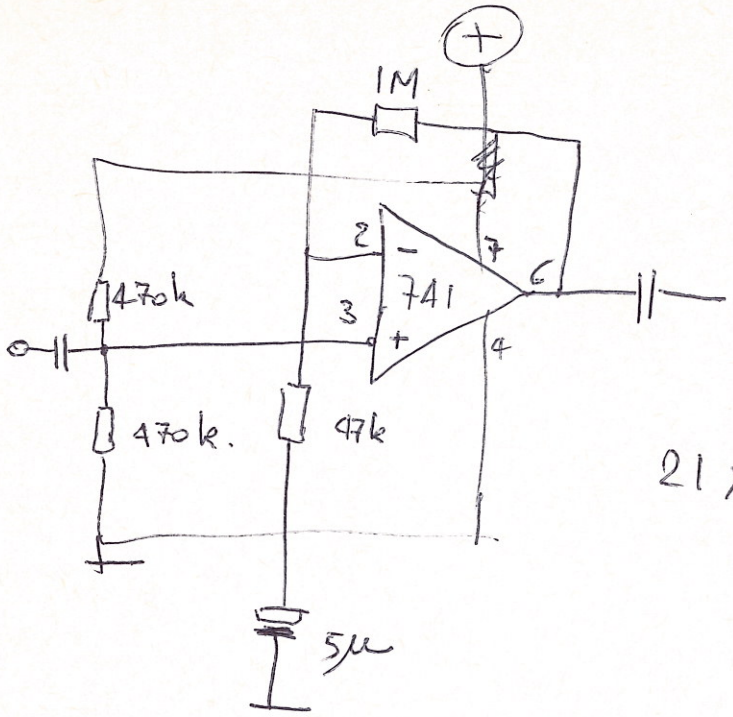
A/D.

LM324

3140

LM 310

Unity gain op-amp.



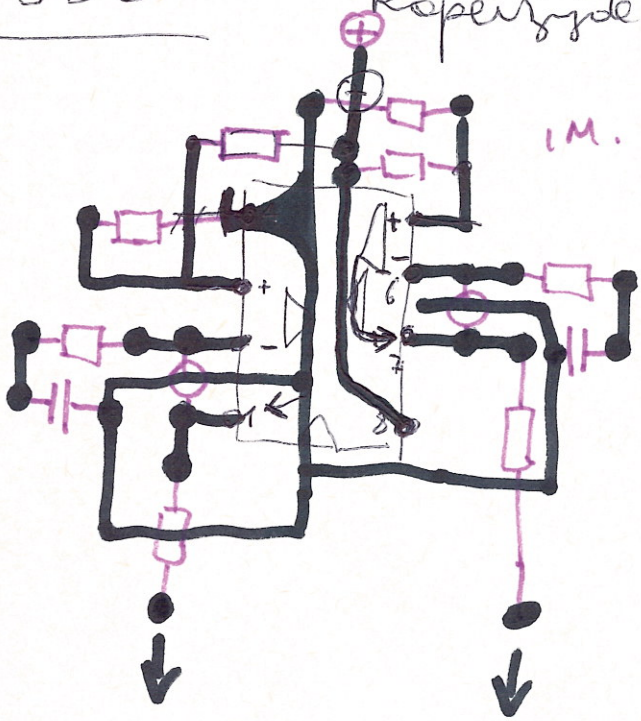
TL081 =

LF351

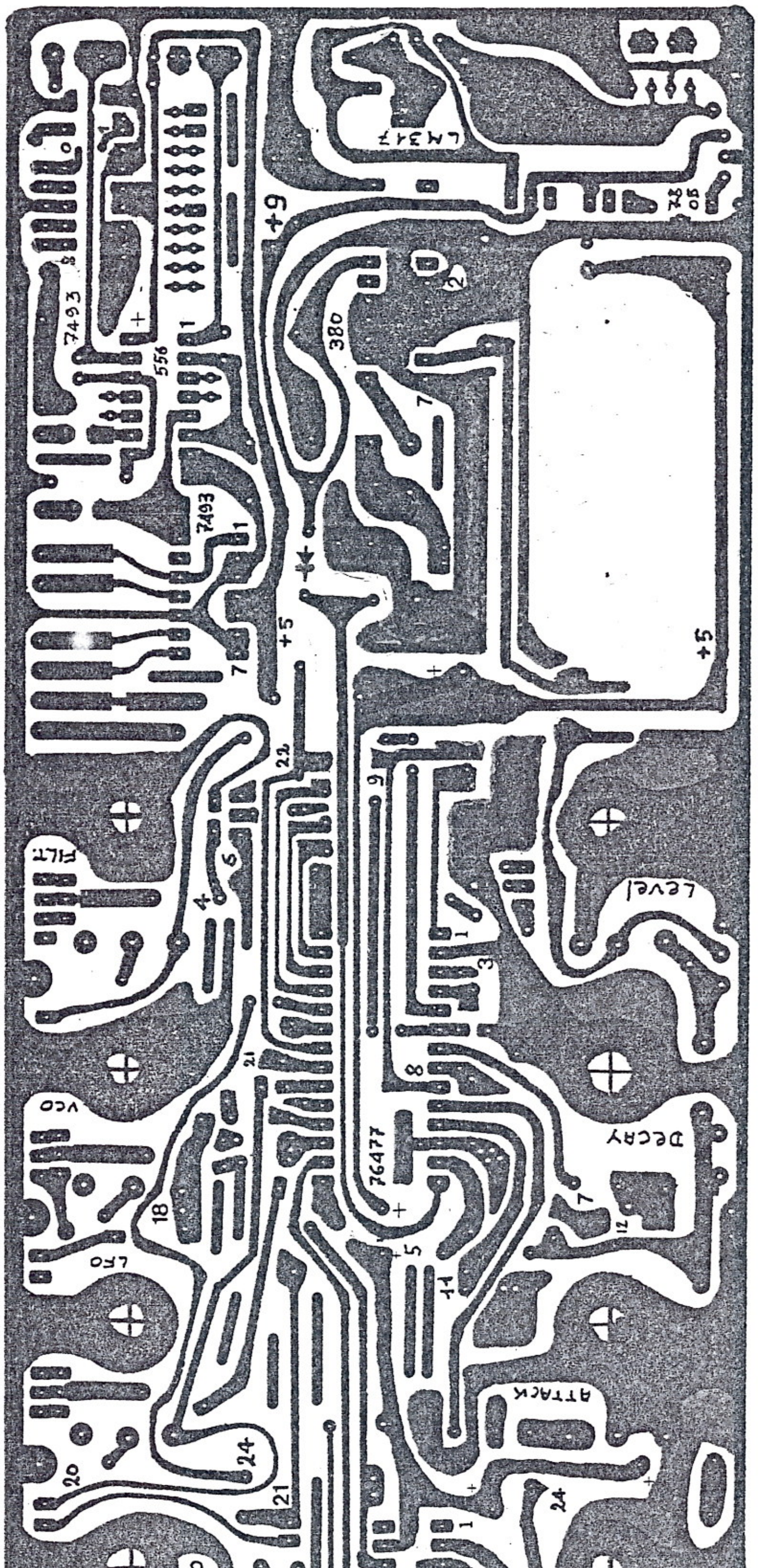
21 x. 2 pin to pin geed voor 741

LF 353

koperzijde print . .

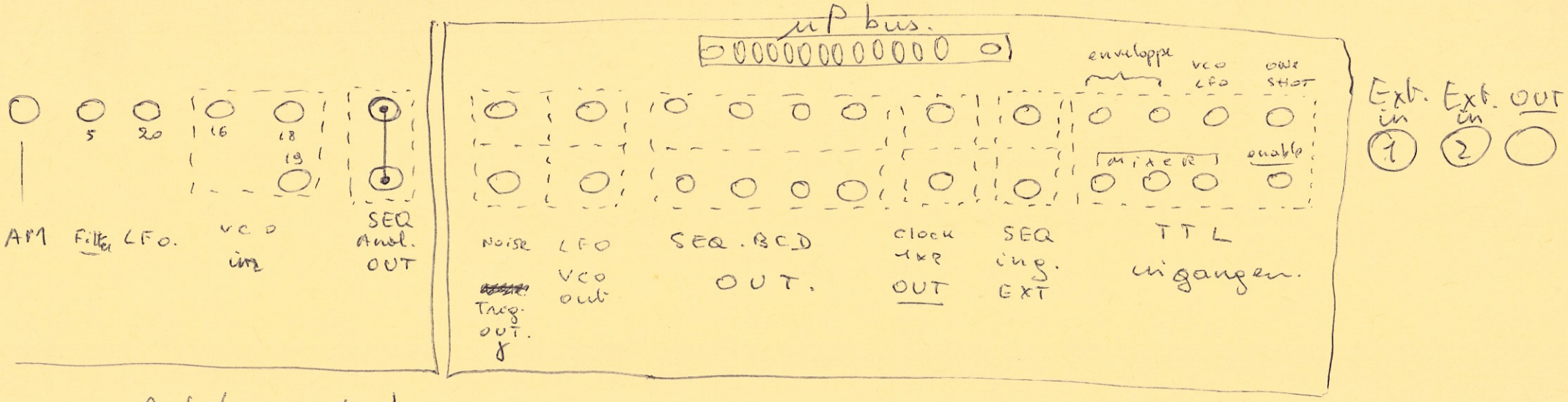


Vooruitwerp



2x gewoon

hard Kontrast



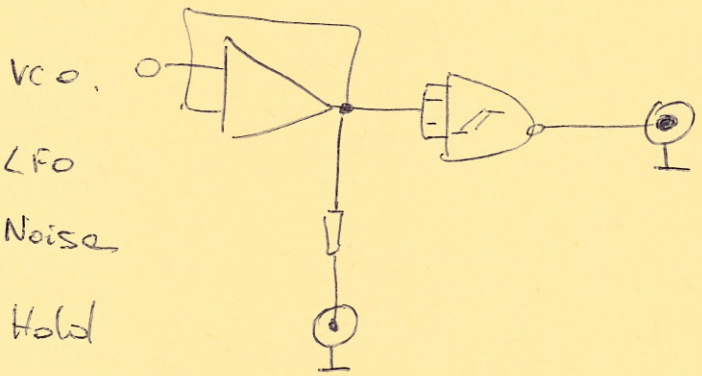
Analog controls. Digitals.

32 pinnen.

III

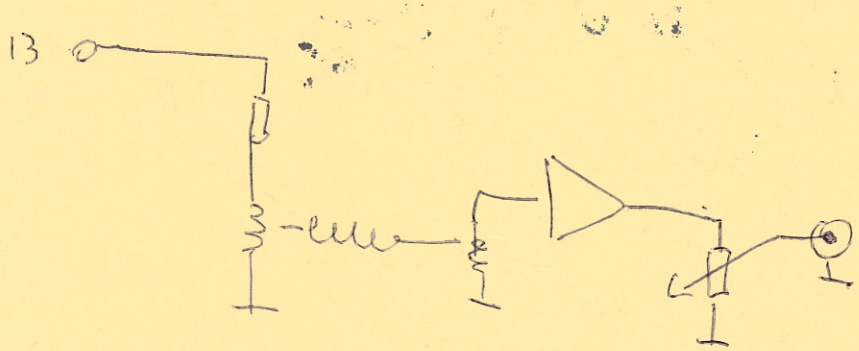
Synthesizer 82.9.

- 2 BCD - sequencers.

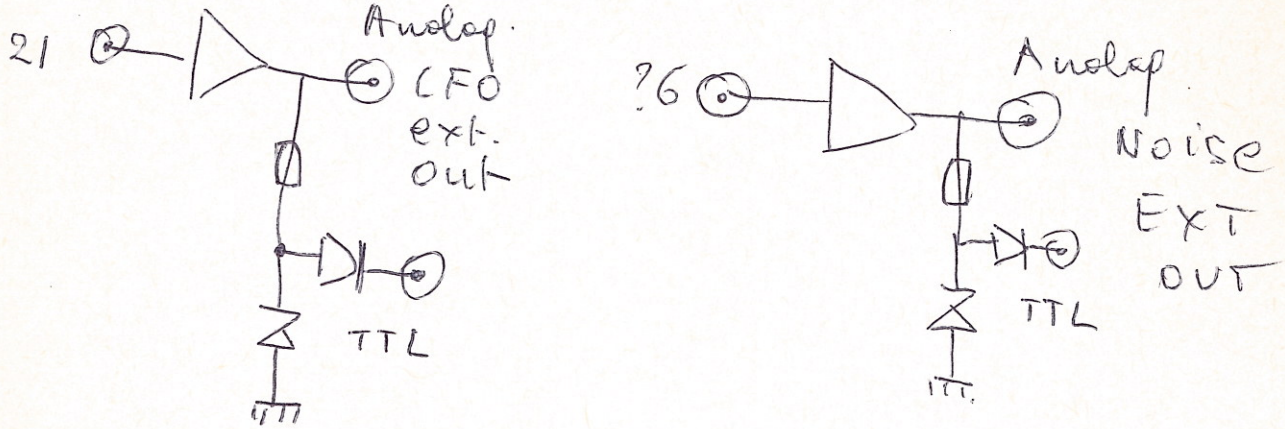


(4 x 741) 1 IC.

2 x 7413.

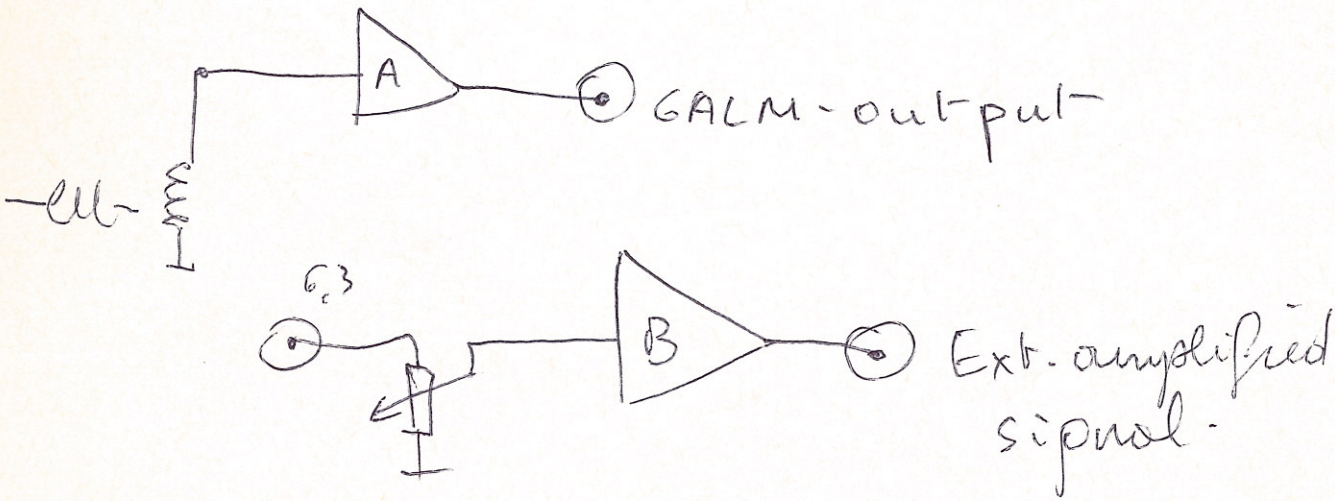


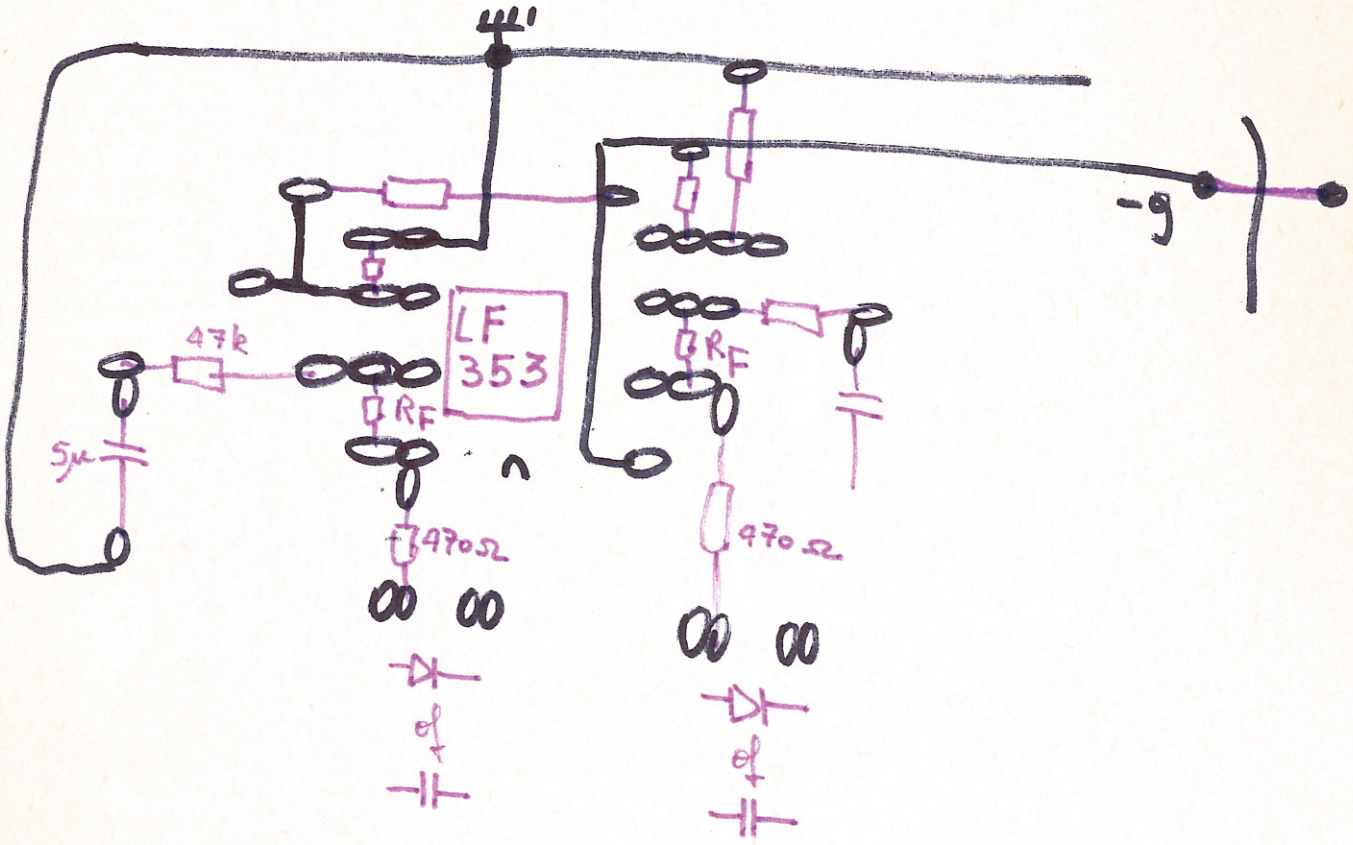
Technische mogelijkheden:



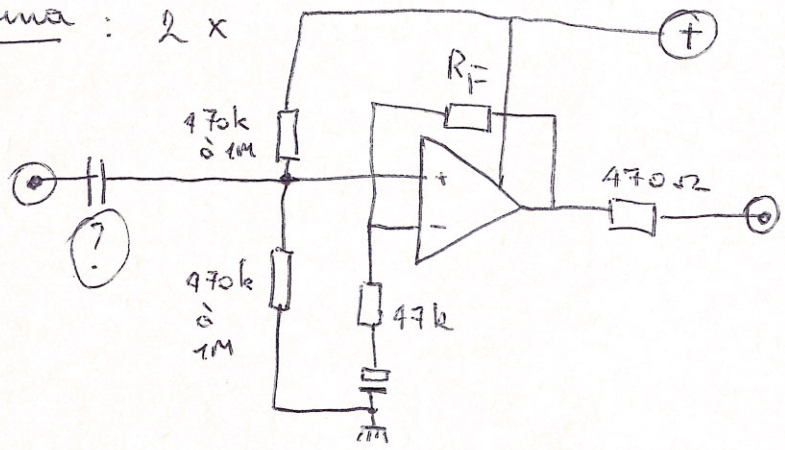
analoog voor - VCO
- Hold
- A/D

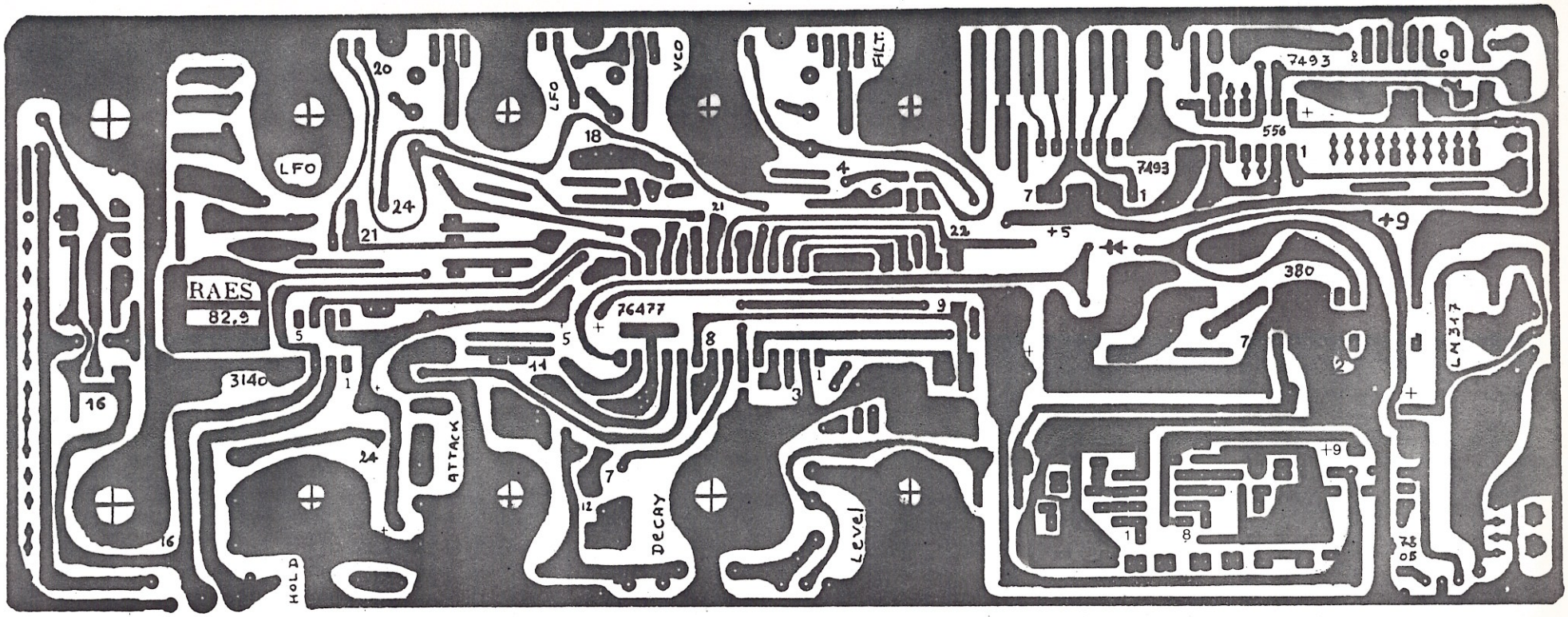
(signaal hoogohmig afvallen over de condensator)





schema : 2 x




RAES
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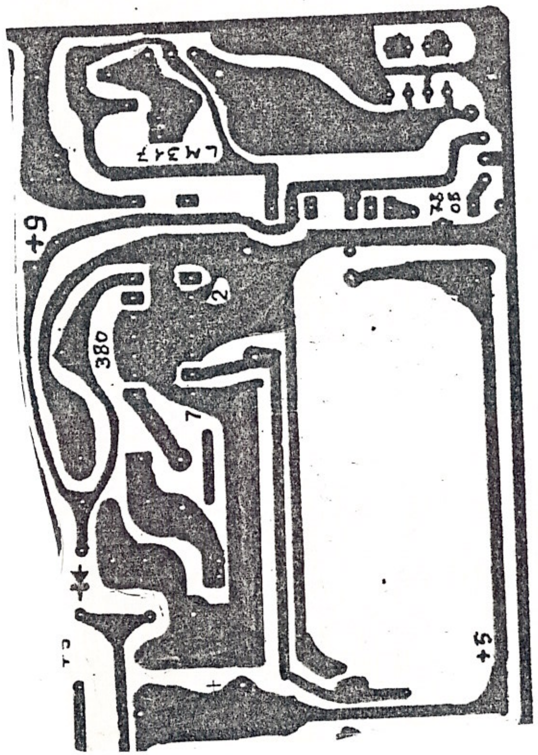


2x
gewoon

hand
Kontrast

Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, L90, and LS90, divide-by-six for the 92A and LS92, and divide-by-eight for the 93A, L93, and LS93.

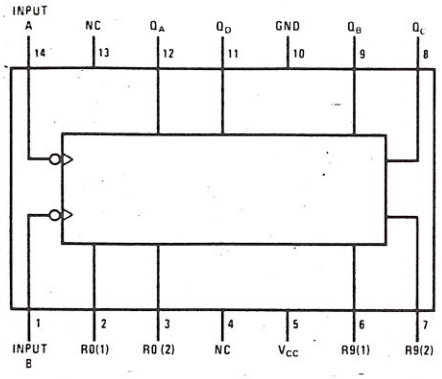
All of these counters have a gated zero reset and the 90A, L90, and LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A, L90, or LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

TYPE	TYPICAL POWER DISSIPATION	COUNT FREQUENCY
90A	145 mW	42 MHz
L90	20 mW	11 MHz
LS90	45 mW	42 MHz
92A, 93A	130 mW	42 MHz
LS92, LS93	45 mW	42 MHz
L93	16 mW	15 MHz

Connection Diagrams



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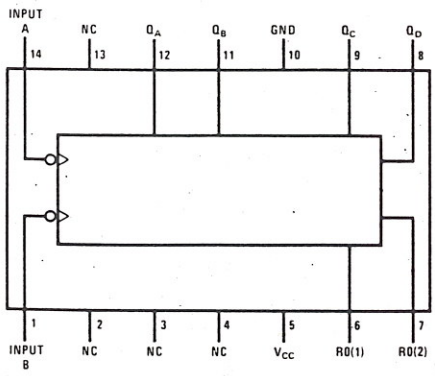
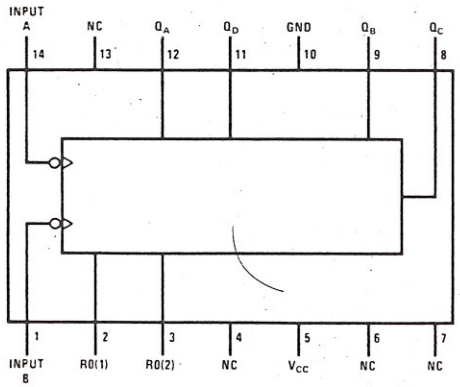
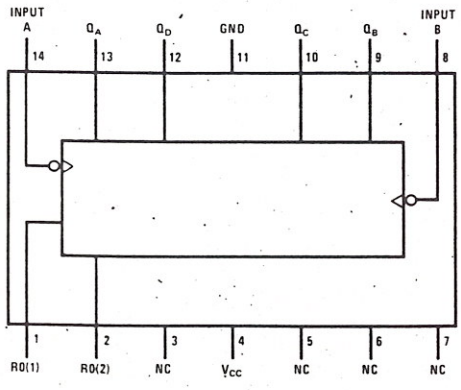
54L90/74L90(J), (N), (W);
54LS90/74LS90(J), (N), (W)



5492A/7492A(J), (N), (W);
54LS92/74LS92(J), (N), (W)



5493A/7493A(J), (N), (W);
54LS93/74LS93(J), (N), (W)



54L93/74L93(J), (N), (W)

LS90, LS92, LS93 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS		DM54/74 90A, 92A, 93A MIN	DM54/74 90A, 92A, 93A TYP(1)	DM54/74 90A, 92A, 93A MAX	DM54L/74L L90, L93 MIN	DM54L/74L L90, L93 TYP(1)	DM54L/74L L90, L93 MAX	DM54LS/74LS LS90, LS92, LS93 MIN	DM54LS/74LS LS90, LS92, LS93 TYP(1)	DM54LS/74LS LS90, LS92, LS93 MAX	UNITS
V_{IH} High Level Input Voltage			2			2			2			V
V_{IL} Low Level Input Voltage		DM54			0.8			0.7			0.7	V
		DM74			0.8			0.7			0.8	

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74									DM54L/74L						UNITS
					90A, LS90			92A, LS92			93A, LS93			L90			L93			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum Count Frequency	A	Q_A	C_L = 50 pF For L90 and L93 C_L = 15 pF For All Others R_L = 400Ω For 90A, 92A and 93A R_L = 2 kΩ For LS90, LS92 and LS93 R_L = 4 kΩ For L90 and L93	32	42		32	42		32	42		6	11		6	15		MHz
		B	Q_B		16			16			16									
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q_A			10	16		10	16		10	16							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12	18		12	18		12	18							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q_D			32	48		32	48		46	70		175	300		210	400	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					34	50		34	50		46	70		190	300		230	400	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_B			10	16		10	16		10	16							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					14	21		14	21		14	21							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_C			21	32		10	16		21	32							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	35		14	21		23	35							
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q_D			21	32		21	32		34	51							ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	35		23	35		34	51							
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Set-to-0	Any			26	40		26	40		26	40							ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Set-to-9	Q_A, Q_D			20	30													ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Q_B, Q_C			26	40													
t_W	Pulse Width	A Input			15			15			15			90			90			ns
		B Input			30			30			30			90			90			
		Reset Input			15			15			15			200			200			
t_{SETUP}	Reset Inactive State Setup Time				25			25			25			200			200			ns

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) Q_A outputs are tested at I_{OL} = max plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

(4) I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS			DM54/74 90A, 92A, 93A			DM54L/74L L90, L93			DM54LS/74LS LS90, LS92, LS93			UNITS
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage					2			2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7			0.7	V
					DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5		N/A					V
				I_I = −18 mA						N/A				−1.5	
I_{OH}	High Level Output Current							−800			−200			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4			2.5	3.4		V
					DM74	2.4	3.4		2.4			2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			2			4	mA
					DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V	I_{OL} = Max (3)	DM54		0.2	0.4		0.15	0.3		0.25	0.4	V
					DM74		0.2	0.4		0.2	0.4		0.35	0.5	
			V_{IL} = Max	I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Any Reset	V_{CC} = Min	V_I = 5.5V				1			0.1				mA
				V_I = 7V										0.1	
		A Input		V_I = 5.5V				1			0.2			0.4	
		B Input		V_I = 5.5V	L90						0.4				
					Others			1			0.2			0.8	
I_{IH}	High Level Input Current	Any Reset	V_{CC} = Max	V_I = 2.7V for LS, V_I = 2.4V for Others				40			10			20	μA
		A Input						80			20			120	
		B Input			93			80			20			40	
					Others			120			40			80	
I_{IL}	Low Level Input Current	Any Reset	V_{CC} = Max	V_I = 0.3V for L, V_I = 0.4V for Others				−1.6			−0.18			−0.4	mA
		A Input						−3.2			−0.36			−2.4	
		B Input			93			−3.2			−0.36			−1.6	
					Others			−4.8			−0.72			−3.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−57	−3	−9	−15	−30		−130	mA
					DM74	−18		−57	−3	−9	−15	−30		−130	
I_{CC}	Supply Current		V_{CC} = Max(4)		90A		29	42							mA
					Others		26	39			5.5		9	15	

Truth Tables

90A, L90, LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A, L90, LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

92A, LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

93A, L93, LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A, L90, LS90
RESET/COUNT TRUTH TABLE

RESET INPUTS R0(1)	R0(2)	R9(1)	R9(2)	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

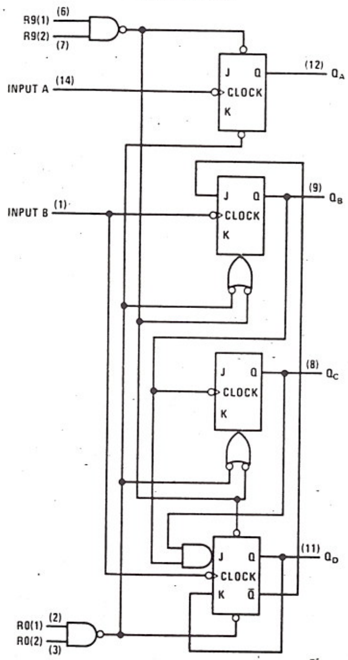
92A, LS92, 93A, L93, LS93
RESET/COUNT TRUTH TABLE

RESET INPUTS R0(1)	R0(2)	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

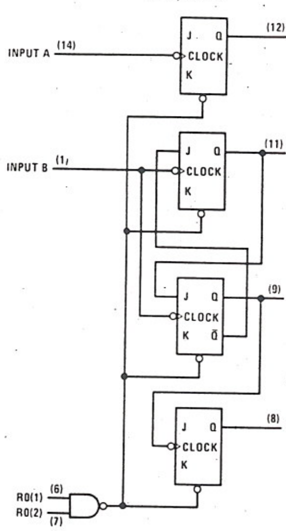
Notes:
(A) Output Q_A is connected to input B for BCD count.
(B) Output Q_D is connected to input A for bi-quinary count.
(C) Output Q_A is connected to input B.
(D) H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams

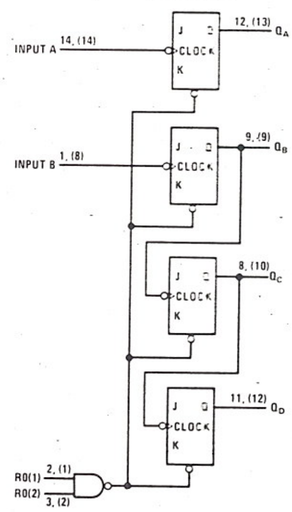
90A, L90, LS90



92A, LS92



93A, L93, LS93



Note: Numbers in parenthesis are for L93 only.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

XR-555
Timing Circuit

GENERAL DESCRIPTION

The XR-555 monolithic timing circuit is a highly stable controller capable of producing accurate timing pulses. It is a direct, pin-for-pin replacement for the SE/NE 555 timer. The circuit contains independent control terminals for triggering or resetting if desired, as shown in the functional block diagram of Figure 1.

In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor (as shown in Figure 2).

The XR-555 may be triggered or reset on falling waveforms. Its output can source or sink up to 200 mA or drive TTL circuits.

FEATURES

- Direct Replacement for SE/NE 555
- Timing from Microseconds Thru Hours
- Operates in Both Monostable and Astable Modes
- High Current Drive Capability (200 mA)
- TTL and DTL Compatible Outputs
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

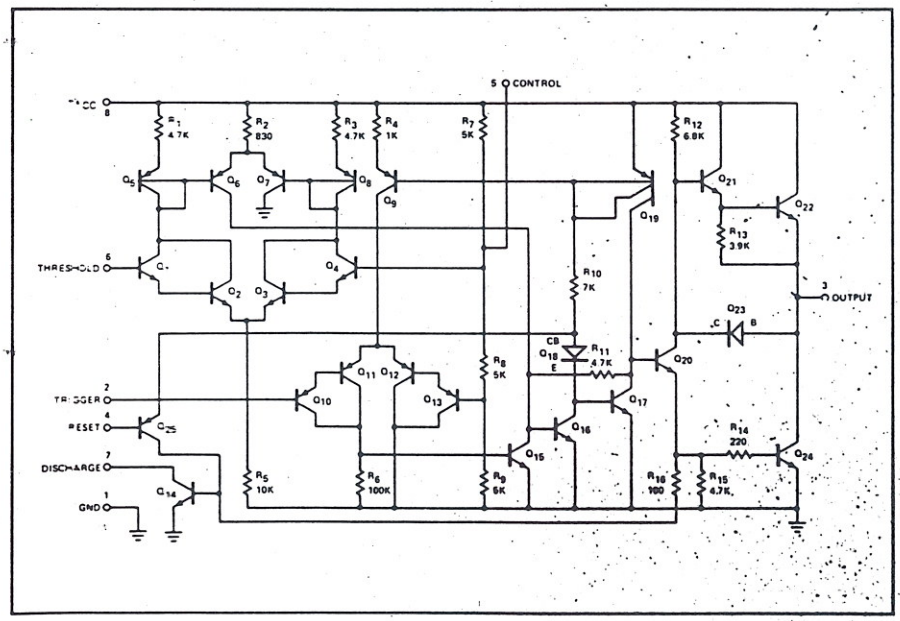
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Pulse Shaping
- Clock Generation
- Missing Pulse Detection
- Pulse-Width Modulation
- Frequency Division
- Pulse-Position Modulation
- Appliance Timing

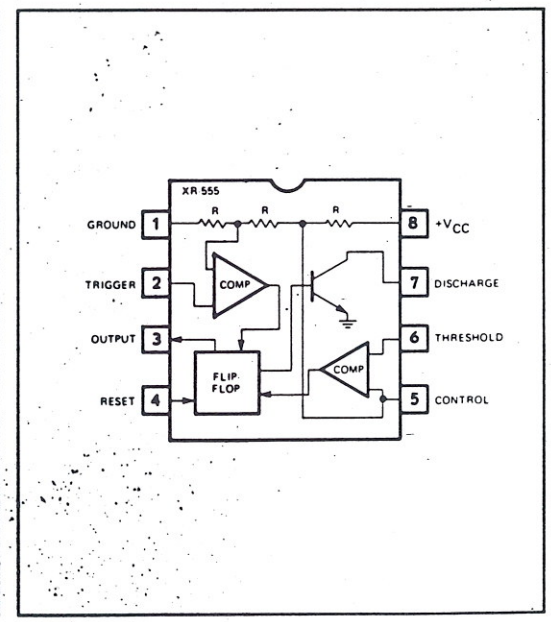
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-555M	Ceramic	−55°C to +125°C
XR-555CM	Ceramic	0°C to +75°C
XR-555CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



XR-556
Dual Timer

GENERAL DESCRIPTION

The XR-556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. It is a direct, pin-for-pin replacement for the SE/NE 556 dual timer. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-556 may be triggered or reset on falling waveforms. Each output can source or sink up to 150 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-556 are superior to those available from two separate timer packages.

FEATURES

- Direct Replacement for SE/NE 556
- Replaces Two 555-Type Timers
- TTL Compatible Pinouts
- Timing from Microseconds Thru Hours
- Excellent Matching Between Timer Sections
- Operates in Both Monostable and Astable Modes
- High Current Drive Capability (150 mA each output)
- TTL and DTL Compatible Outputs
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

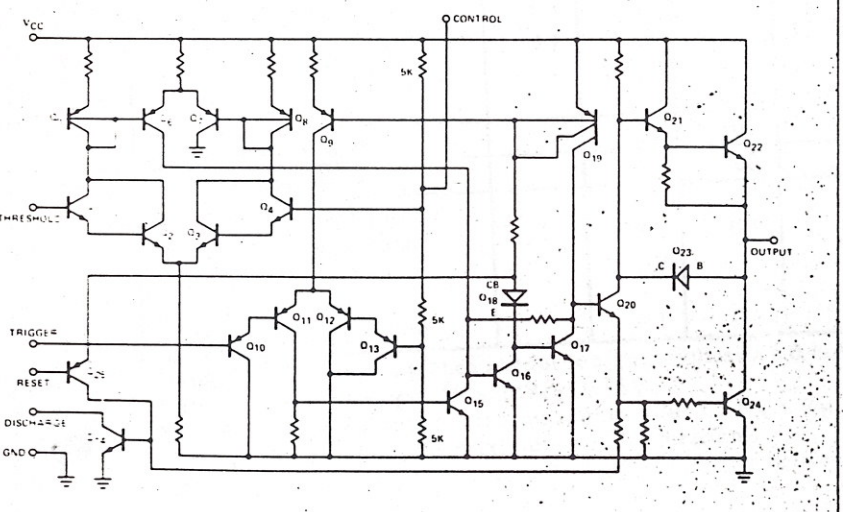
APPLICATIONS

Precision Timing	Missing Pulse Detection
Pulse Generation	Pulse-Width Modulation
Sequential Timing	Frequency Division
Pulse Shaping	Clock Synchronization
Time Delay Generation	Pulse-Position Modulation
Clock Pattern Generation	Appliance Timing

AVAILABLE TYPES

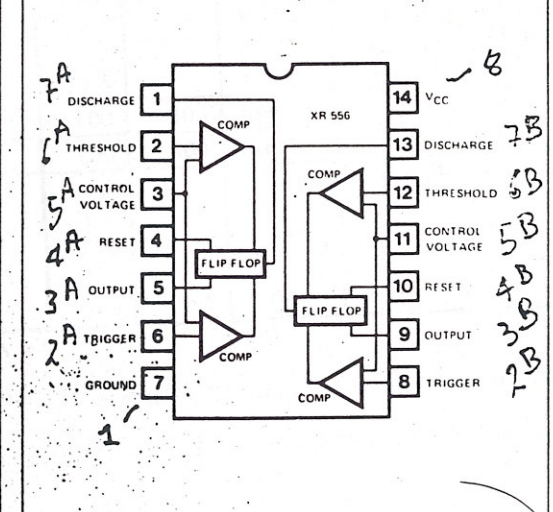
Part Number	Package	Operating Temperature
XR-556M	Ceramic	−55°C to +125°C
XR-556CN	Ceramic	0°C to +75°C
XR-556CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



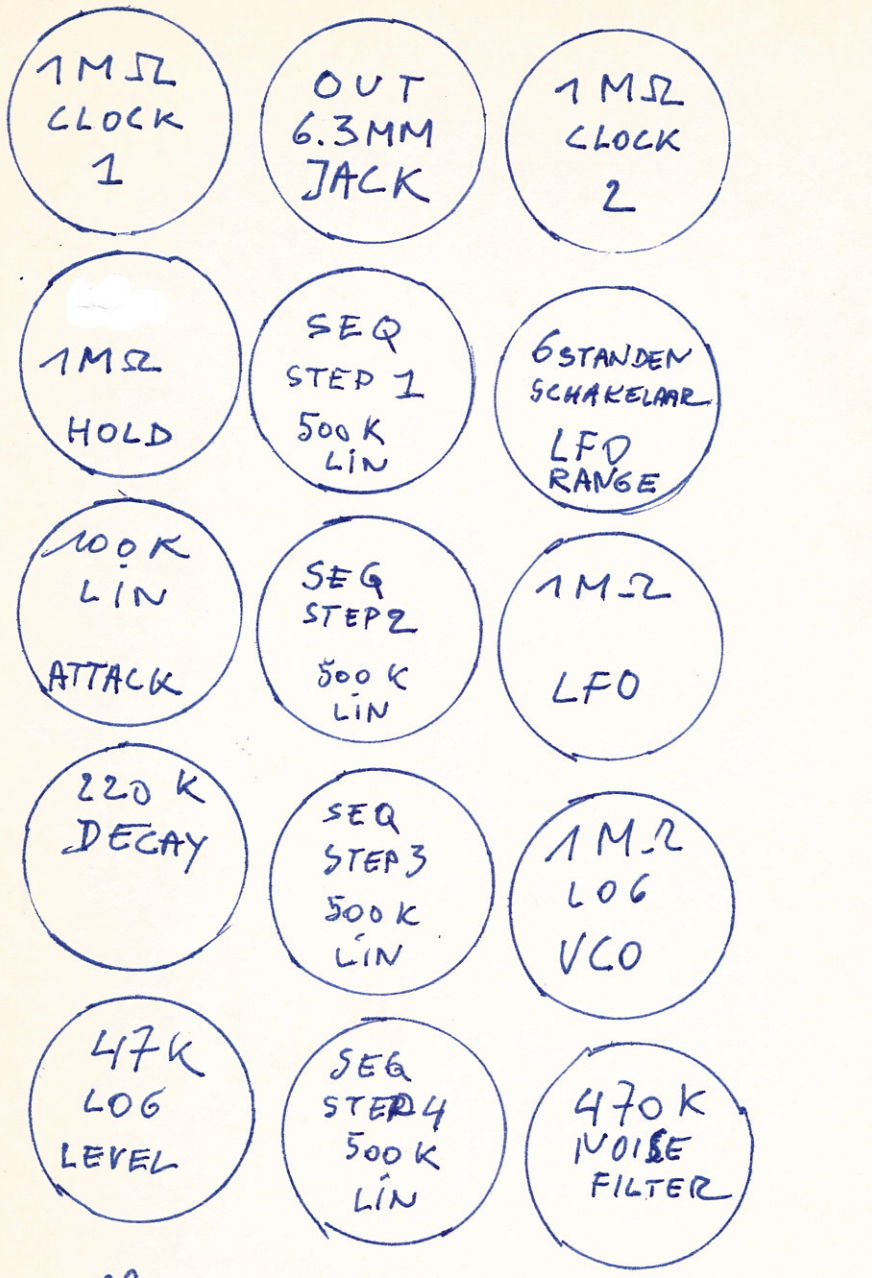
One Section of XR-556

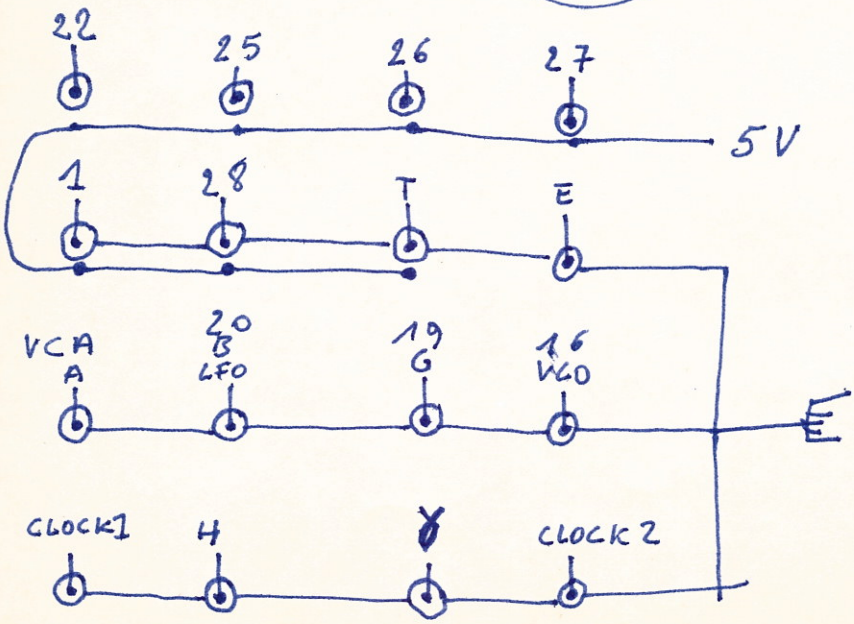
FUNCTIONAL BLOCK DIAGRAM



SYNTHE LOG voor José van den Broucke

Frontplaat

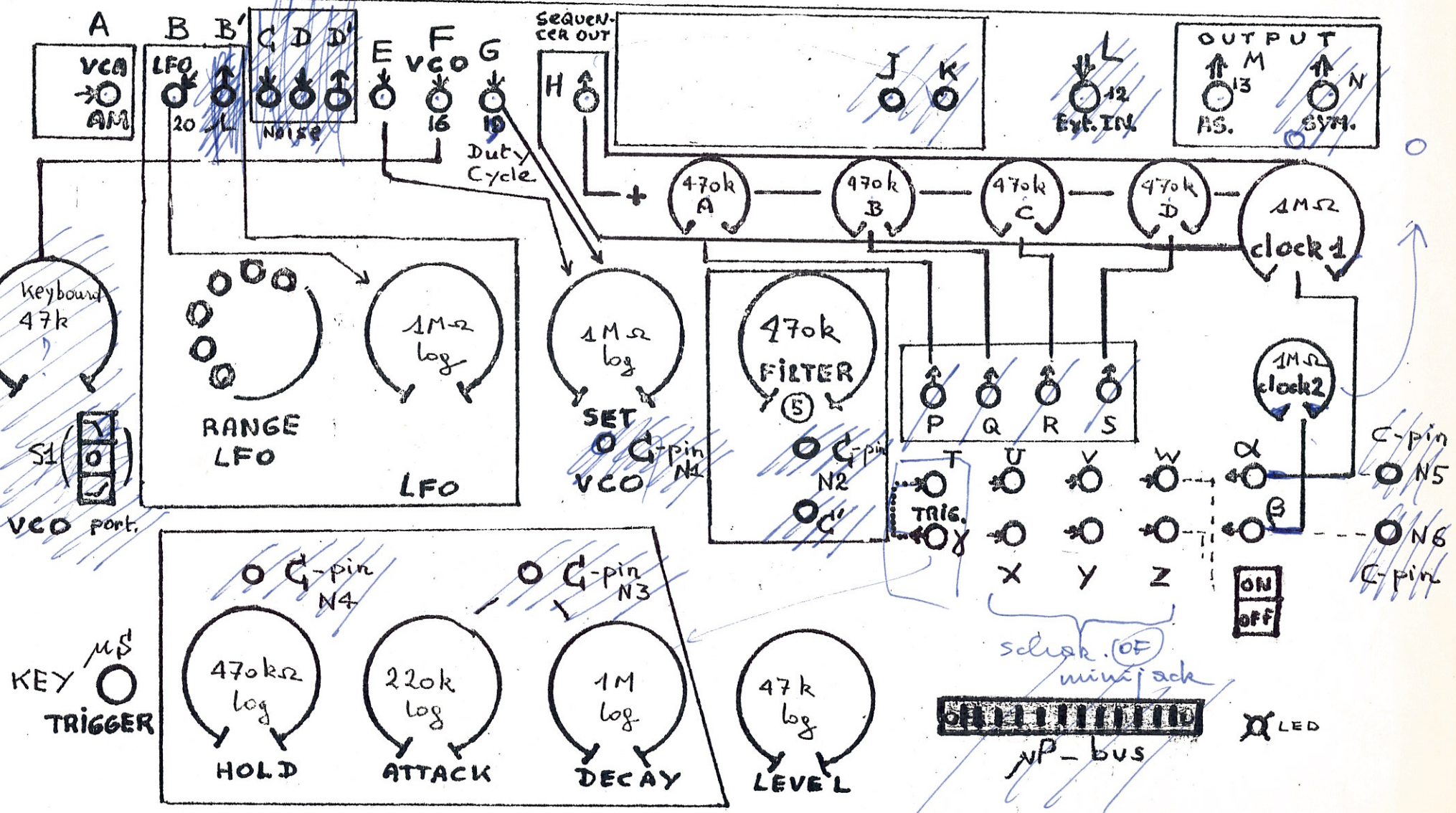




Synthelog III
82/3

5 exemplaren : verkocht; boeverpakketten

SYNTHELOG III



6.3.

XR-555

Timing Circuit

GENERAL DESCRIPTION

The XR-555 monolithic timing circuit is a highly stable controller capable of producing accurate timing pulses. It is a direct, pin-for-pin replacement for the SE/NE 555 timer. The circuit contains independent control terminals for triggering or resetting if desired, as shown in the functional block diagram of Figure 1.

In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor (as shown in Figure 2).

The XR-555 may be triggered or reset on falling waveforms. Its output can source or sink up to 200 mA or drive TTL circuits.

FEATURES

- Direct Replacement for SE/NE 555
- Timing from Microseconds Thru Hours
- Operates in Both Monostable and Astable Modes
- High Current Drive Capability (200 mA)
- TTL and DTL Compatible Outputs
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	–65°C to +125°C

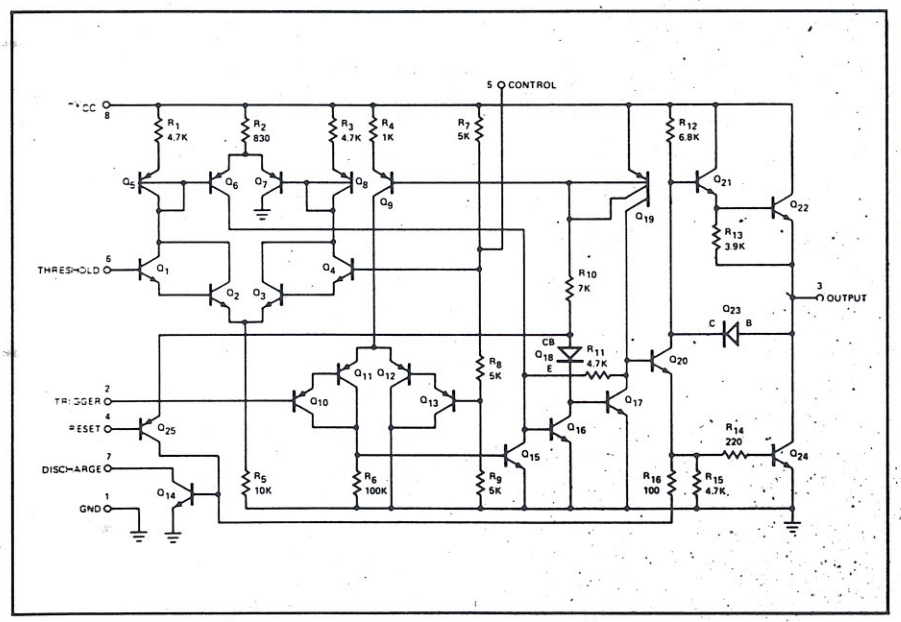
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Pulse Shaping
- Clock Generation
- Missing Pulse Detection
- Pulse-Width Modulation
- Frequency Division
- Pulse-Position Modulation
- Appliance Timing

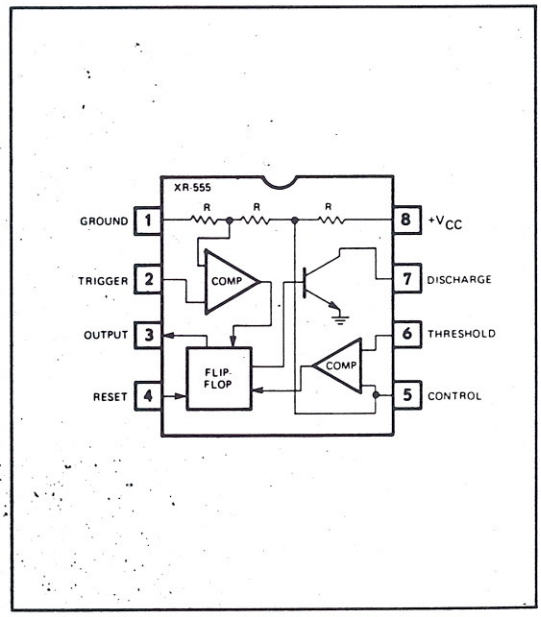
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-555M	Ceramic	–55°C to +125°C
XR-555CM	Ceramic	0°C to +75°C
XR-555CP	Plastic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, L90, and LS90, divide-by-six for the 92A and LS92, and divide-by-eight for the 93A, L93, and LS93.

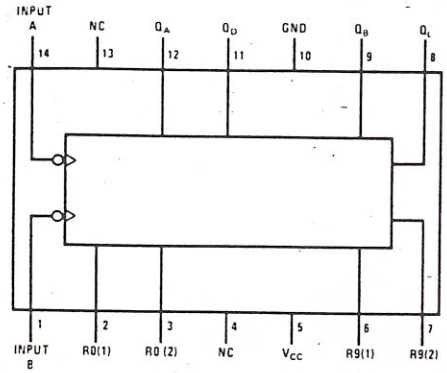
All of these counters have a gated zero reset and the 90A, L90, and LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A, L90, or LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

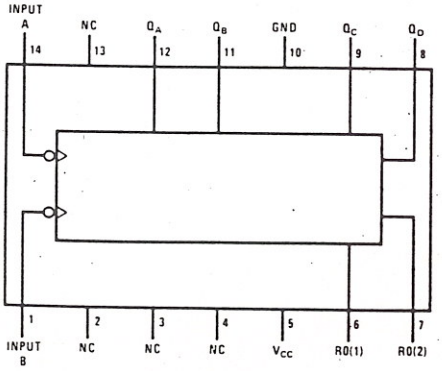
Features

TYPE	TYPICAL POWER DISSIPATION	COUNT FREQUENCY
90A	145 mW	42 MHz
L90	20 mW	11 MHz
LS90	45 mW	42 MHz
92A, 93A	130 mW	42 MHz
LS92, LS93	45 mW	42 MHz
L93	16 mW	15 MHz

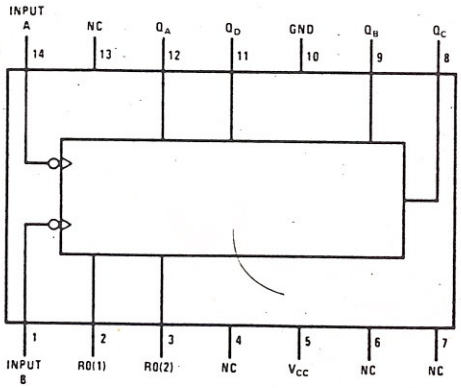
Connection Diagrams



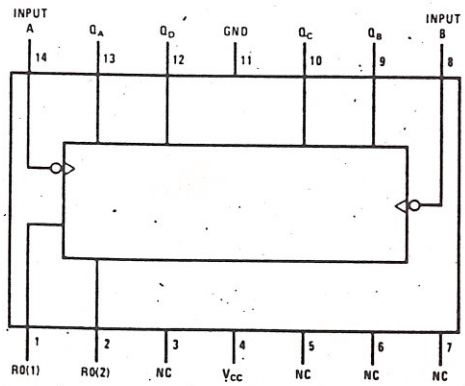
5490A/7490A(J), (N), (W);
54L90/74L90(J), (N), (W);
54LS90/74LS90(J), (N), (W)



5492A/7492A(J), (N), (W);
54LS92/74LS92(J), (N), (W)



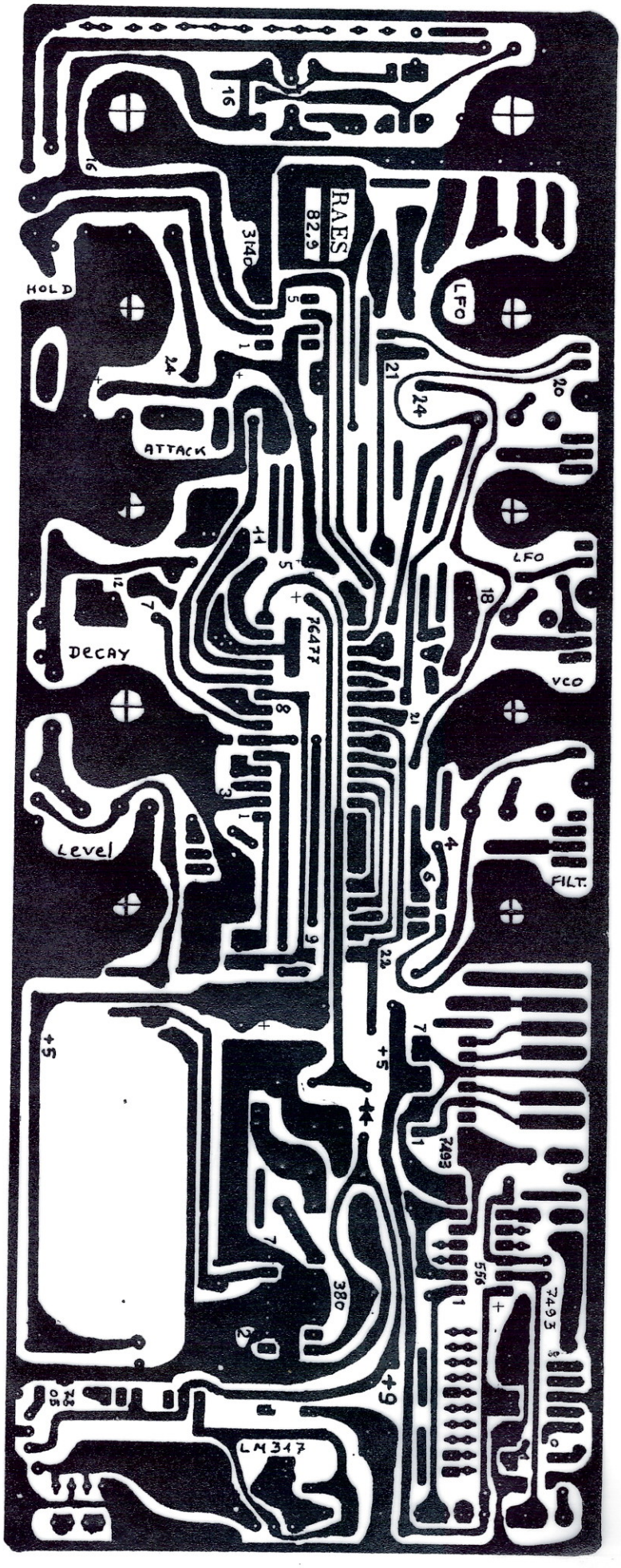
5493A/7493A(J), (N), (W);
54LS93/74LS93(J), (N), (W)



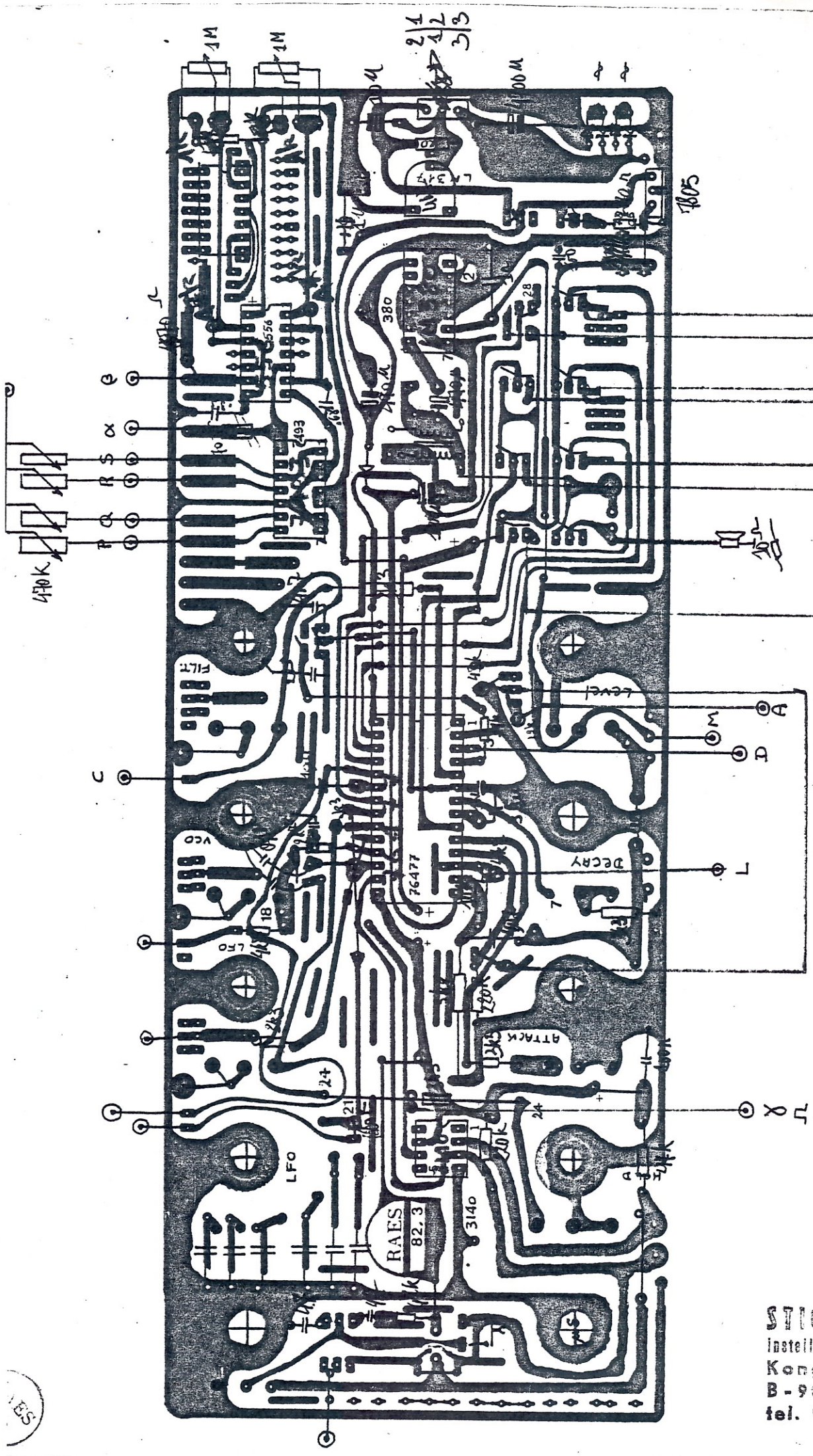
54L93/74L93(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS		DM54/74 90A, 92A, 93A			DM54L/74L L90, L93			DM54LS/74LS LS90, LS92, LS93			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.7			0.7	V
			DM74			0.8			0.7			0.8	


RAES
82.9
HOLD
ATTACK
DECAY
Level
LFO
LFO
VCO
FILT.
LM317
7493
556
380
76477
+5
+9

LM317
KV
000



Stichting Logos
instelling van openbaar nut
afdeling: Vormingswerk

Kongostraat 35

9000 GENT
tel.:(091)23.80.89

KURSUS: Synthesiserbouw - SYNTHELOG

Programma:

1. Inleiding & aansluiting bij algemene elektronikaontwerpkursus

2. Introduktie film : 'Elektronische hilfsmittel zur elektronische klanggestaltung" (16mm film , 30')

3. Wat is een synthesiser ? Een definitorische en historische diskussie.
   - van studio elektronische muziek naar live-elektronics
   - miniaturisatie & modulaire opbouw
   - enkel chip synthesisers : Synthelog

   definitie: een synthesiser is een elektronisch toestel waarmee klanken kunnen worden voortgebracht die in hun akoestische eigenschappen door de gebruiker kunnen worden bepaald bij middel van spanningssturing of digitale programmatie.

   - dwz: een speelautomaat is géén synthesiser omdat de geluiden niét door de speler worden bepaald.
   - spanningssturing of digitale programmatie: kontrole van parameters zonder ingreep in de hardware van het toestel.

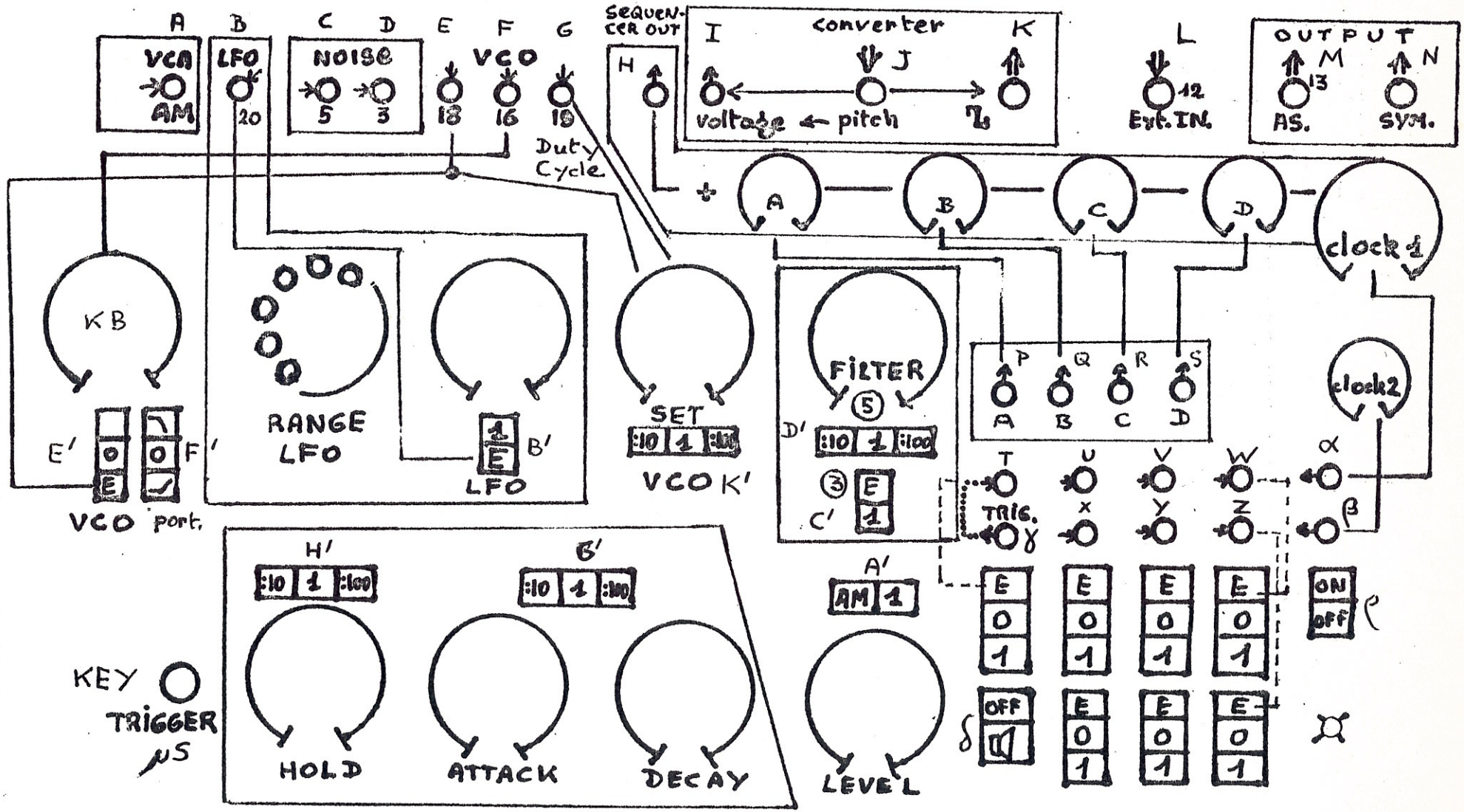
Kontroleerbare parameters :		
	frekwentie = toonhoogte	logaritmisch verband !
	intensiteit= volume	id.
	klankkleur	diskontinu verband
	plaats	lineair verband
	tijdsduur	lineair verband

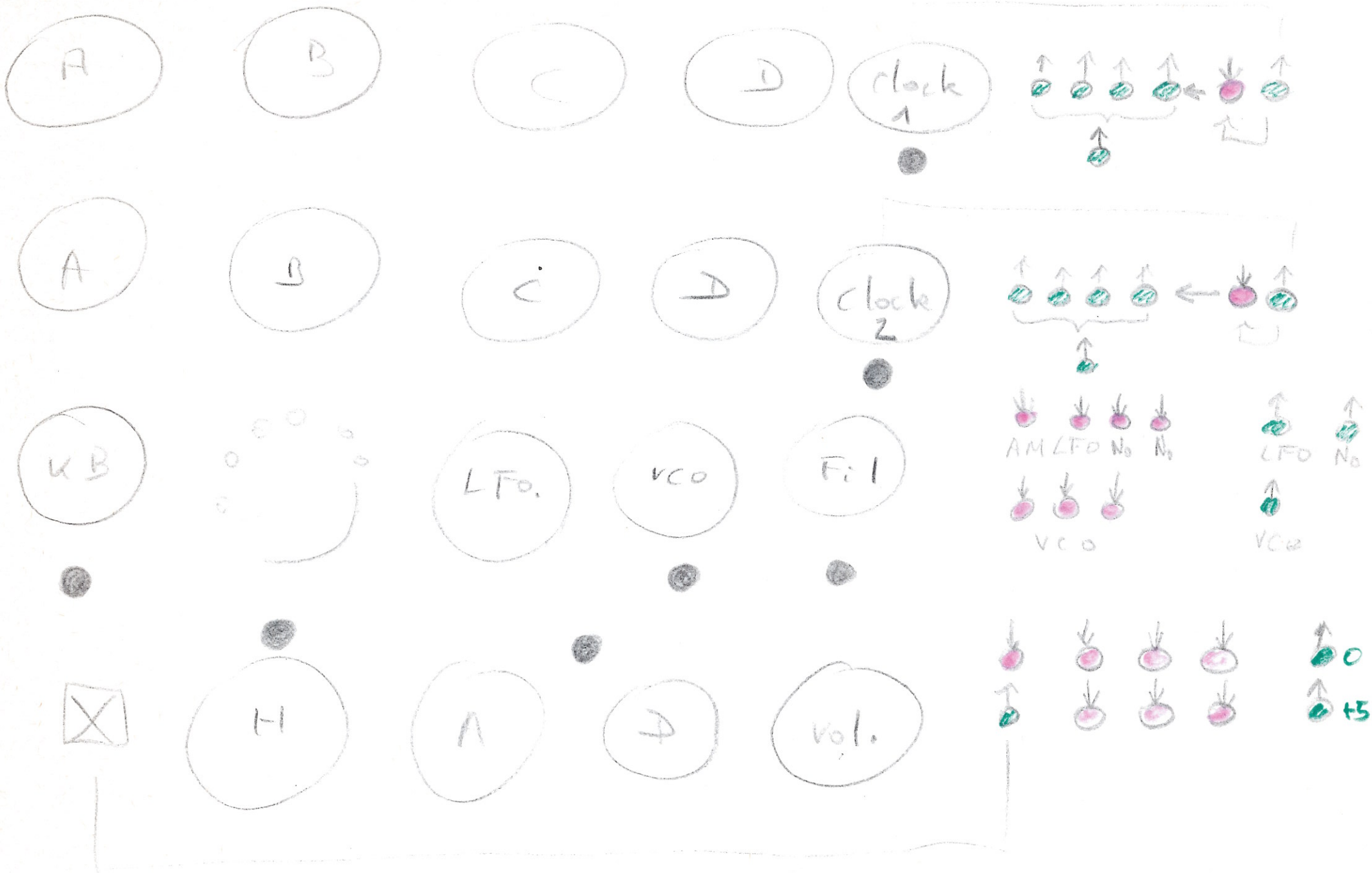
4. Diskussie van kommerciele synthesisers en elektronische orgels : waarden

5. Opzet van de miniatuur-synthesiser SYNTHELOG : enkel-chip concept. Diskussie van de chip : SN 76744 - operationele voorwaarden.

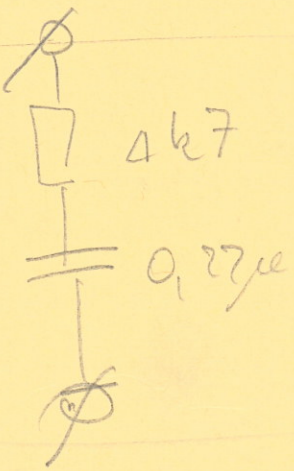
Prijslijst.

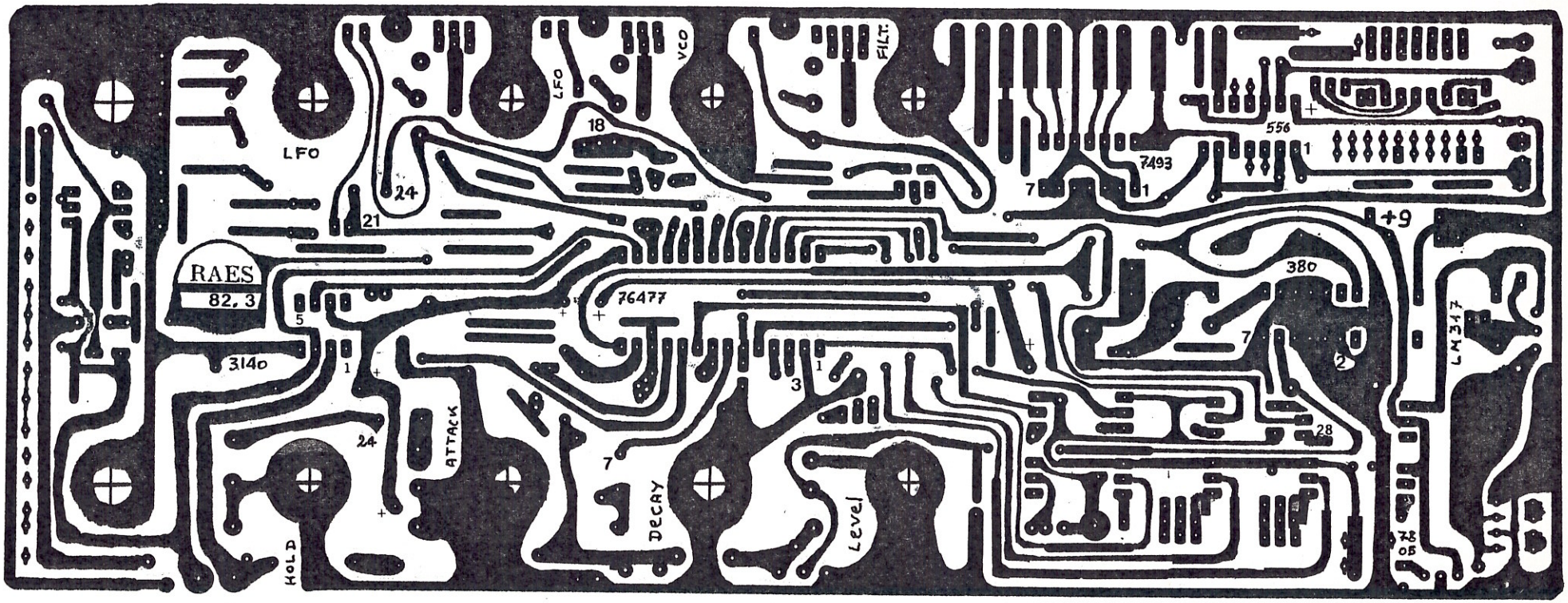
* Synthesizer preset		550,-
* IC	76477	200,-


A
B
C
D
E
F
G
VCA
AM
LFO
20
NOISE
5
3
18
16
19
VCO
Duty Cycle
SEQUENCER OUT
H
I
converter
J
K
voltage
pitch
L
12
Ext. IN.
OUTPUT
M
N
13
AS.
SYM.
KB
RANGE
LFO
LFO
SET
VCO
FILTER
5
clock1
clock2
P
Q
R
S
T
U
V
W
α
β
TRIG.
X
Y
Z
γ
δ
ON
OFF
E'
F'
B'
K'
D'
C'
A'
H'
G'
VCO port.
KEY
TRIGGER
HOLD
ATTACK
DECAY
LEVEL


A
B
C
D
clock 1
A
B
C
D
clock 2
KB
LFO.
VCO
Fil
AM LFO No No
VCO
LFO No
VCO
H
A
D
Vol.
0
+5

LM380	70
556	60
(= 7557 CMOS	108)
3140	22
7493	20
7674	200 à 300
LM317	
7805	




LFO
LFO
VCO
FILT.
18
24
21
7493
556
+9
380
RAES
82. 3
3140
76477
ATTACK
DECAY
Level
HOLD
LM317
28

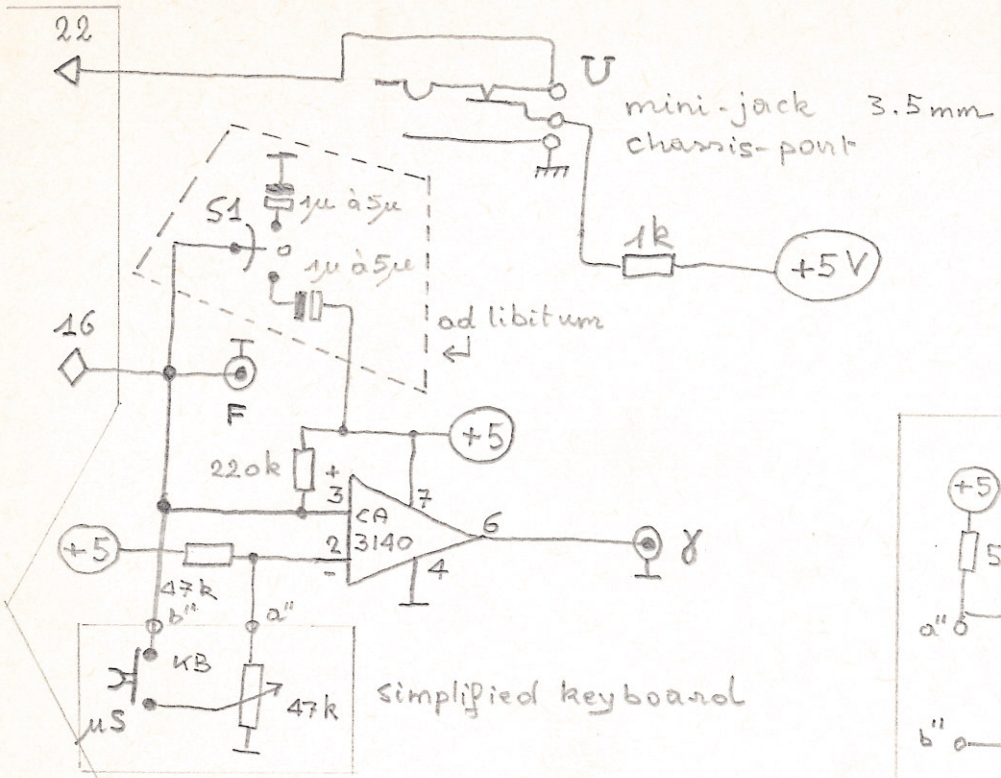
SYNTHELOG III 82.3

bouw en instruktieboek

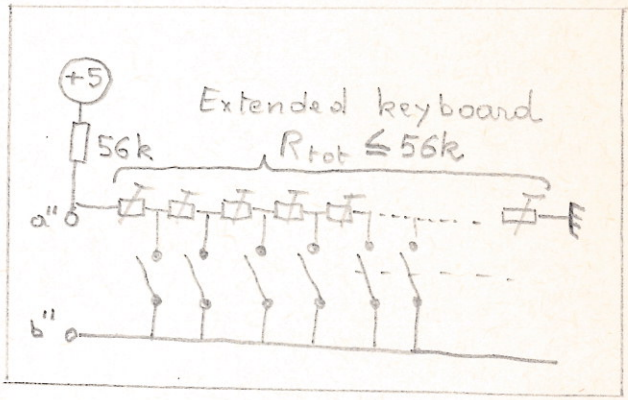
M A S T E R

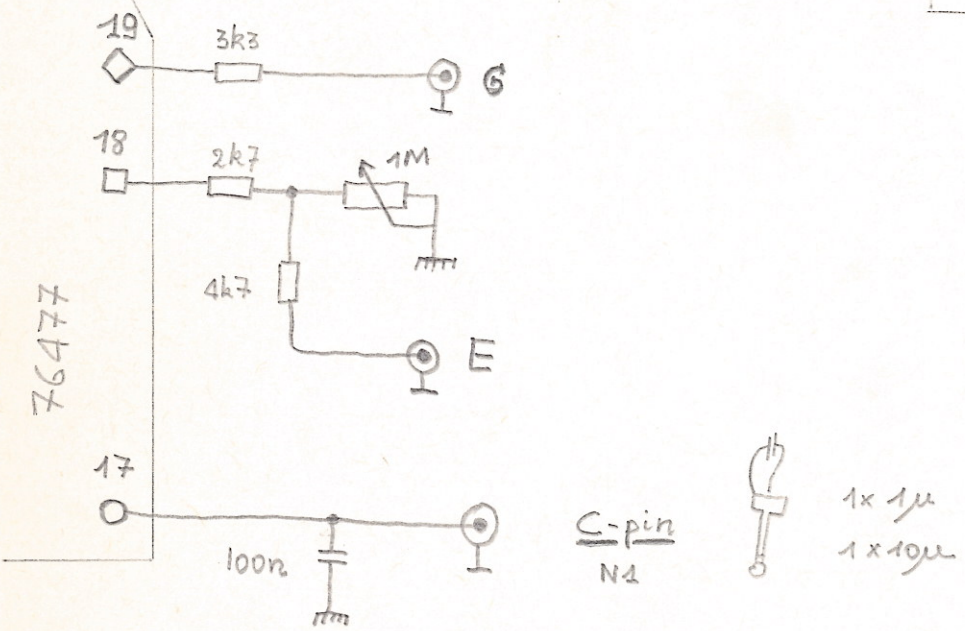
- 5 exemplaren.

VCO



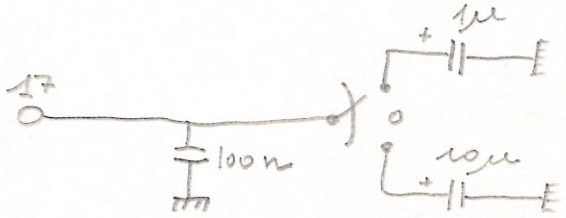
ZONDER PIN : logisch 1
MET PIN : logisch 0
MET PIN & DRAAD : Extern





76477

OR :



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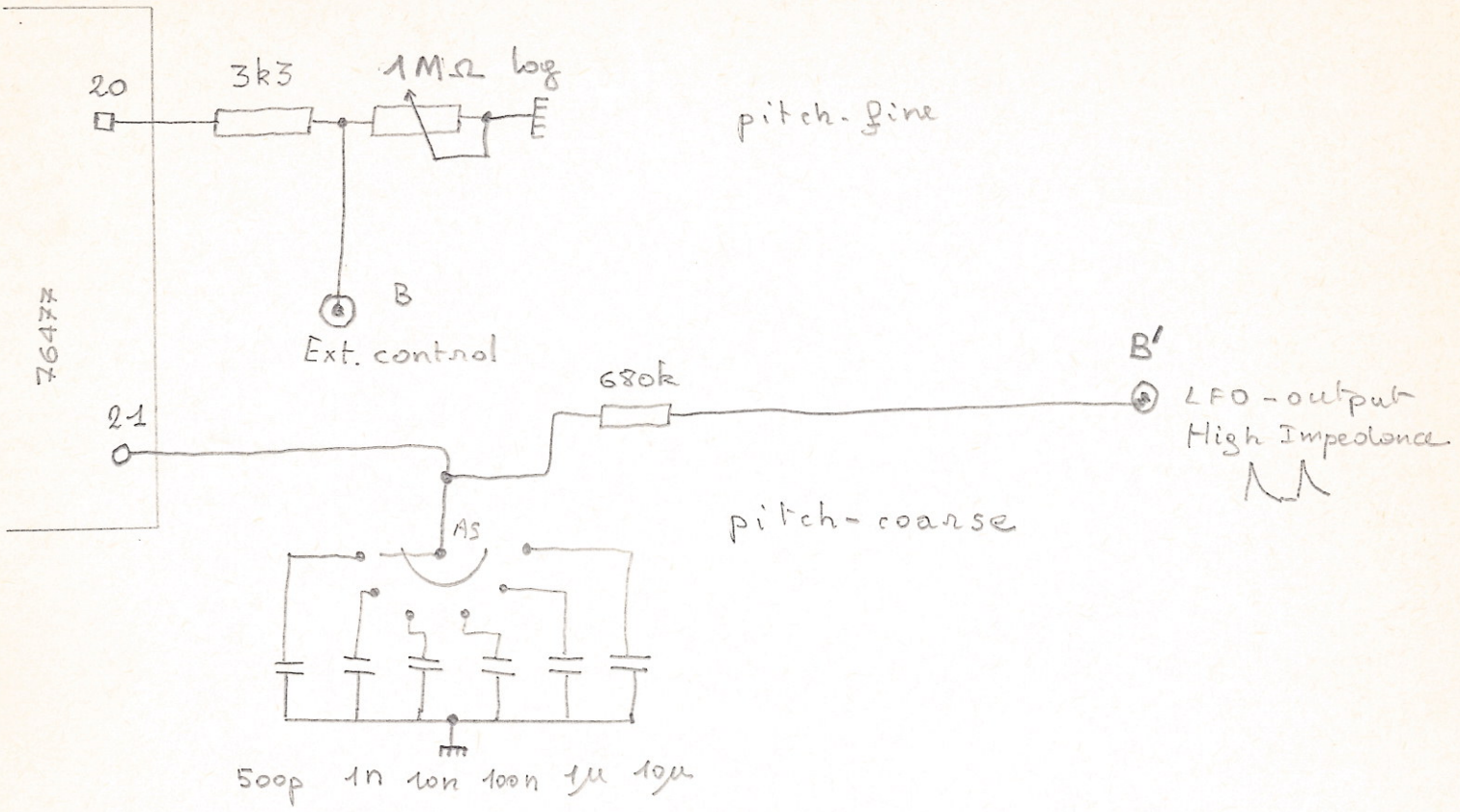
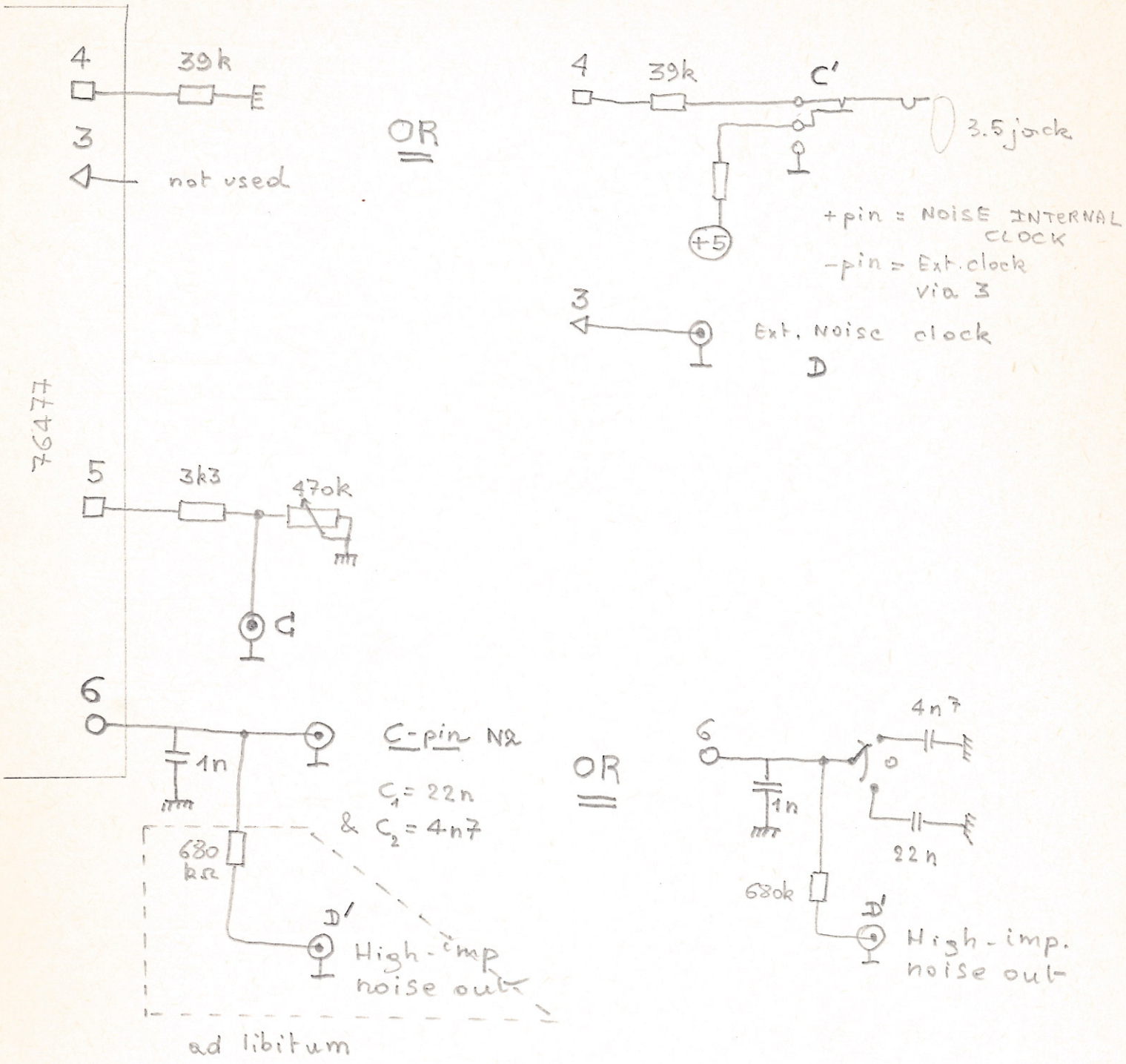
Instelling van openbaar nut
Kongostraat 35
B-9000 Gent
tel. 091-23.80.89

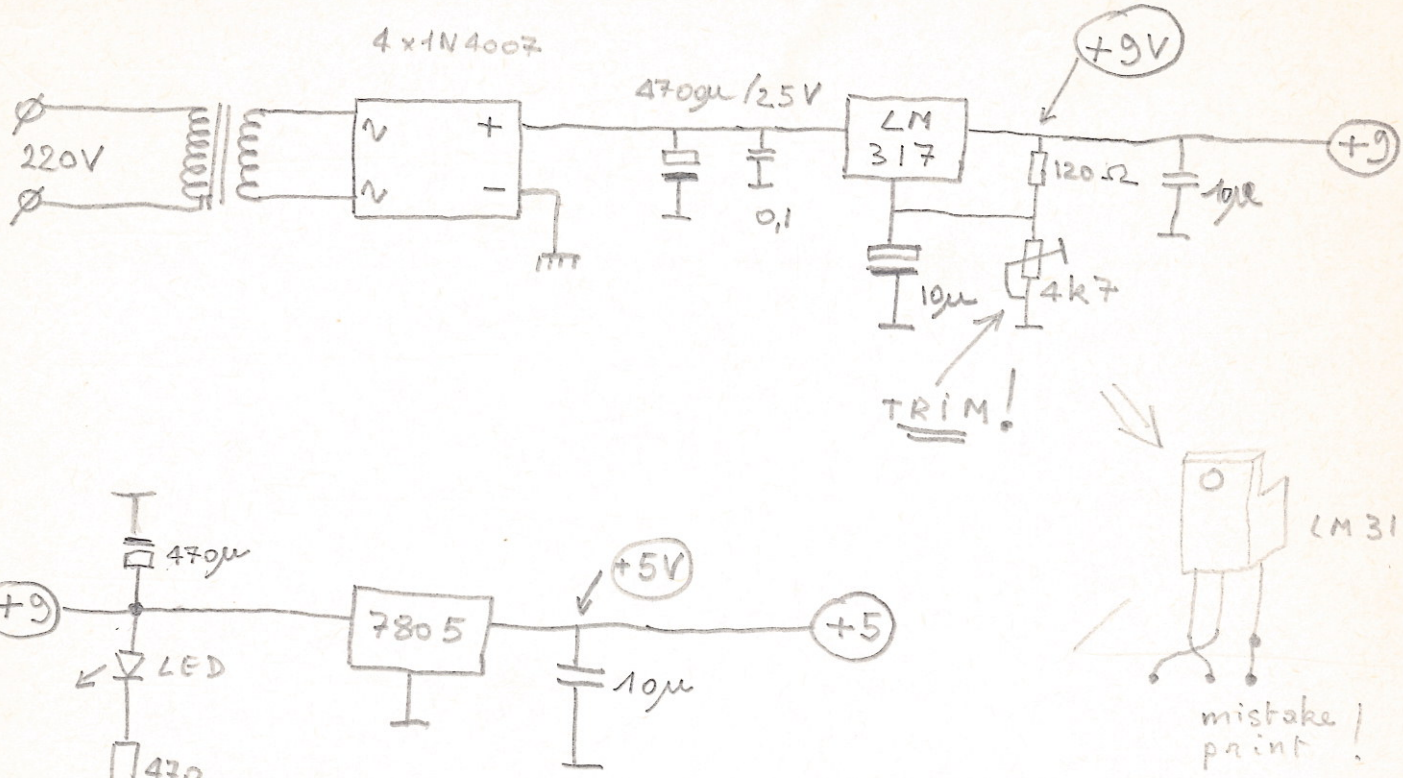
LFO

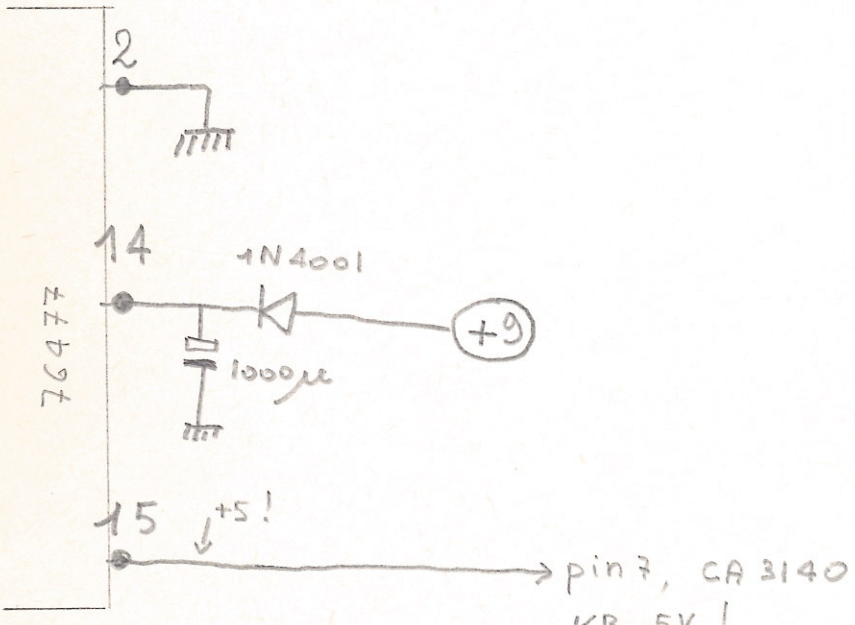


NOISE & FILTER



POWER SUPPLY





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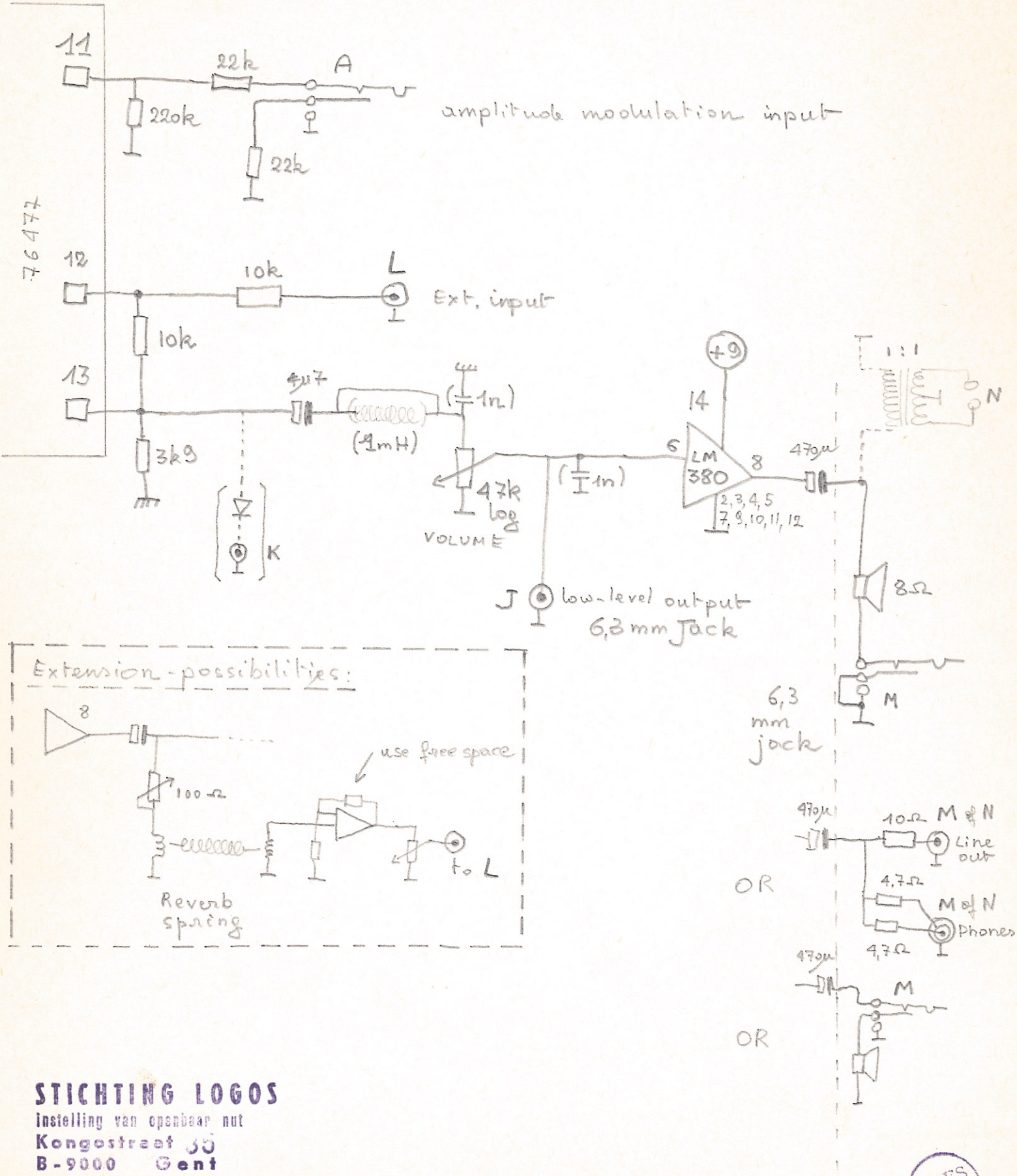
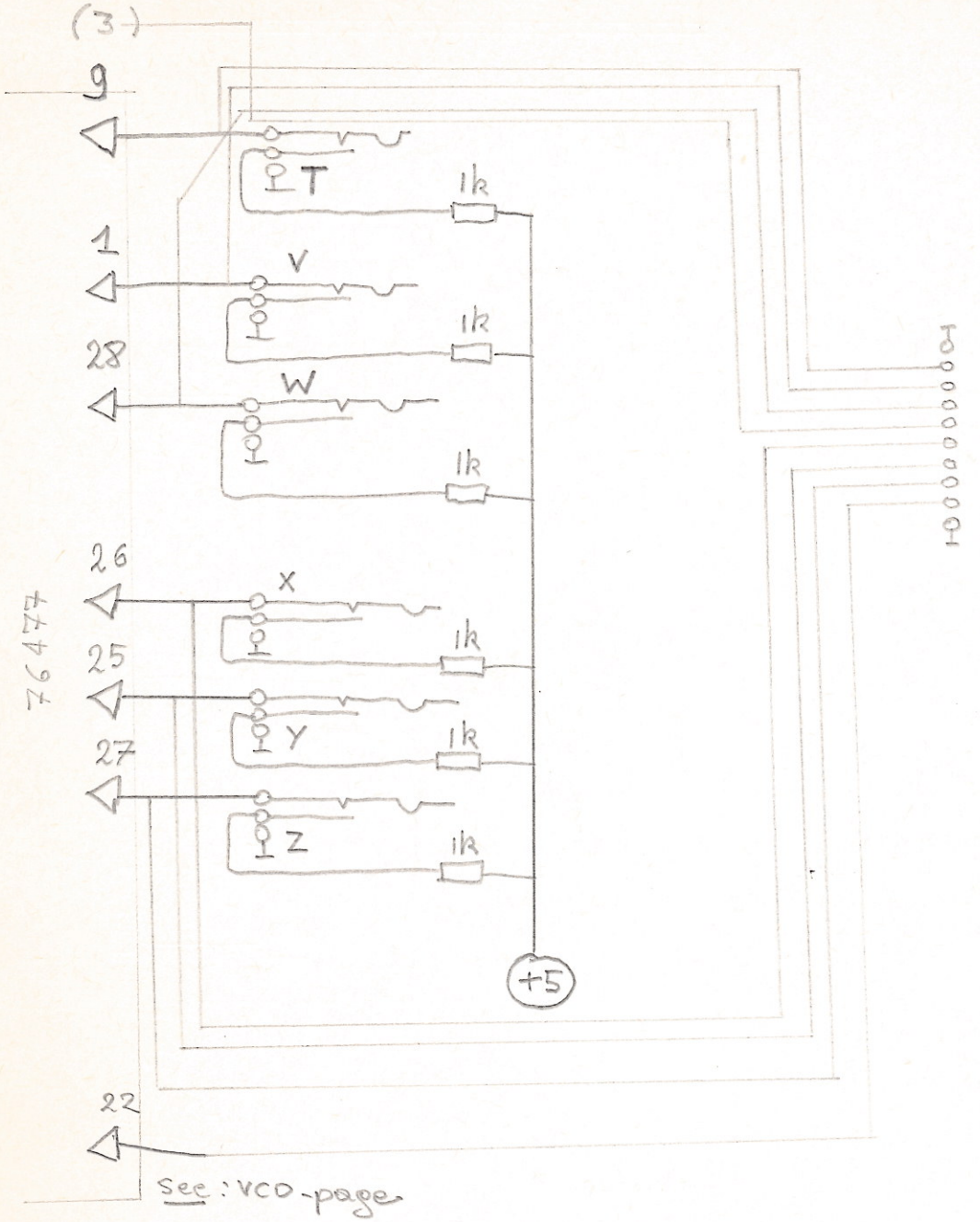
B-9000 Gent
tel. 091-23.80.89

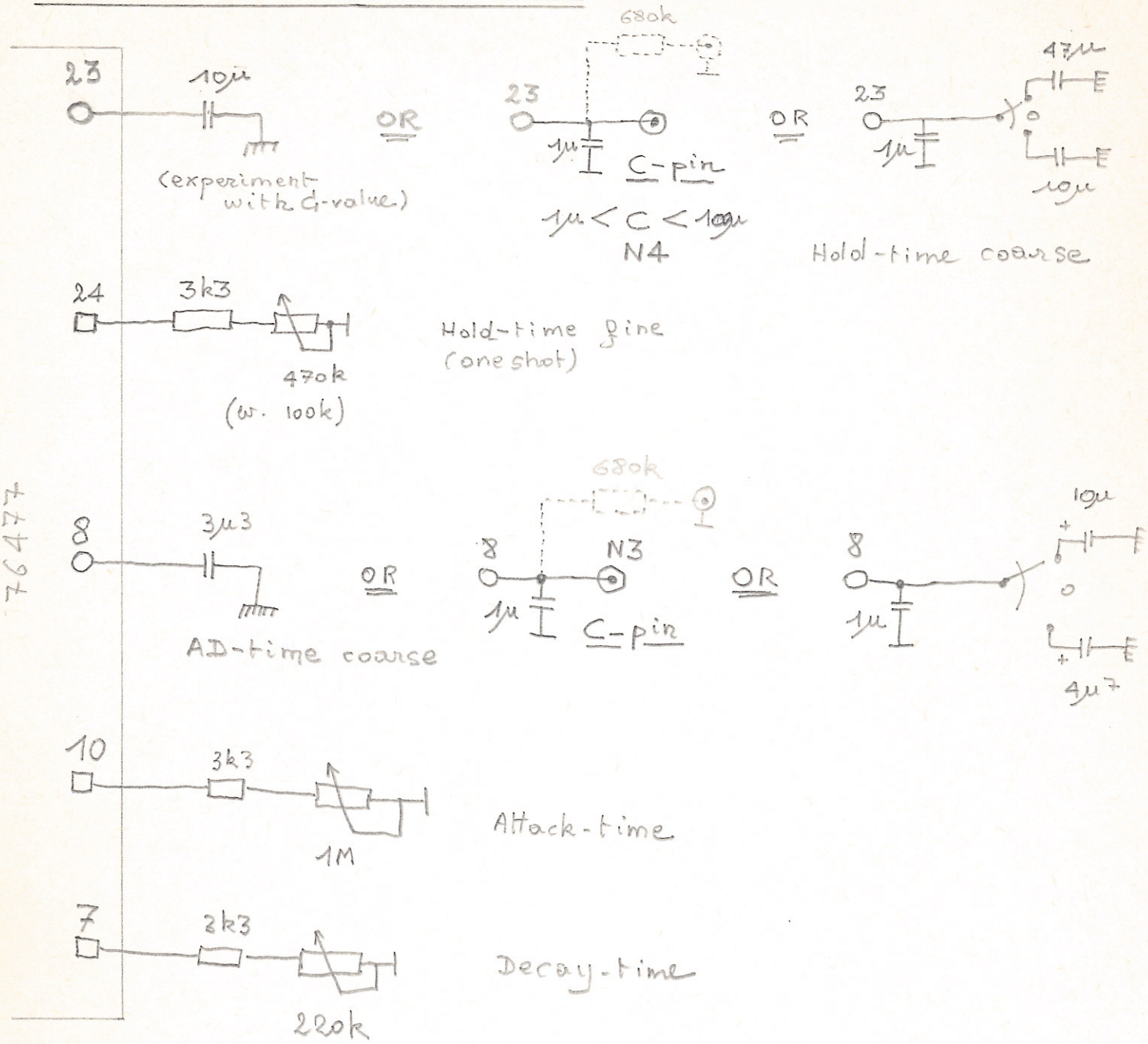
OUTPUT OP-AMP /VCA



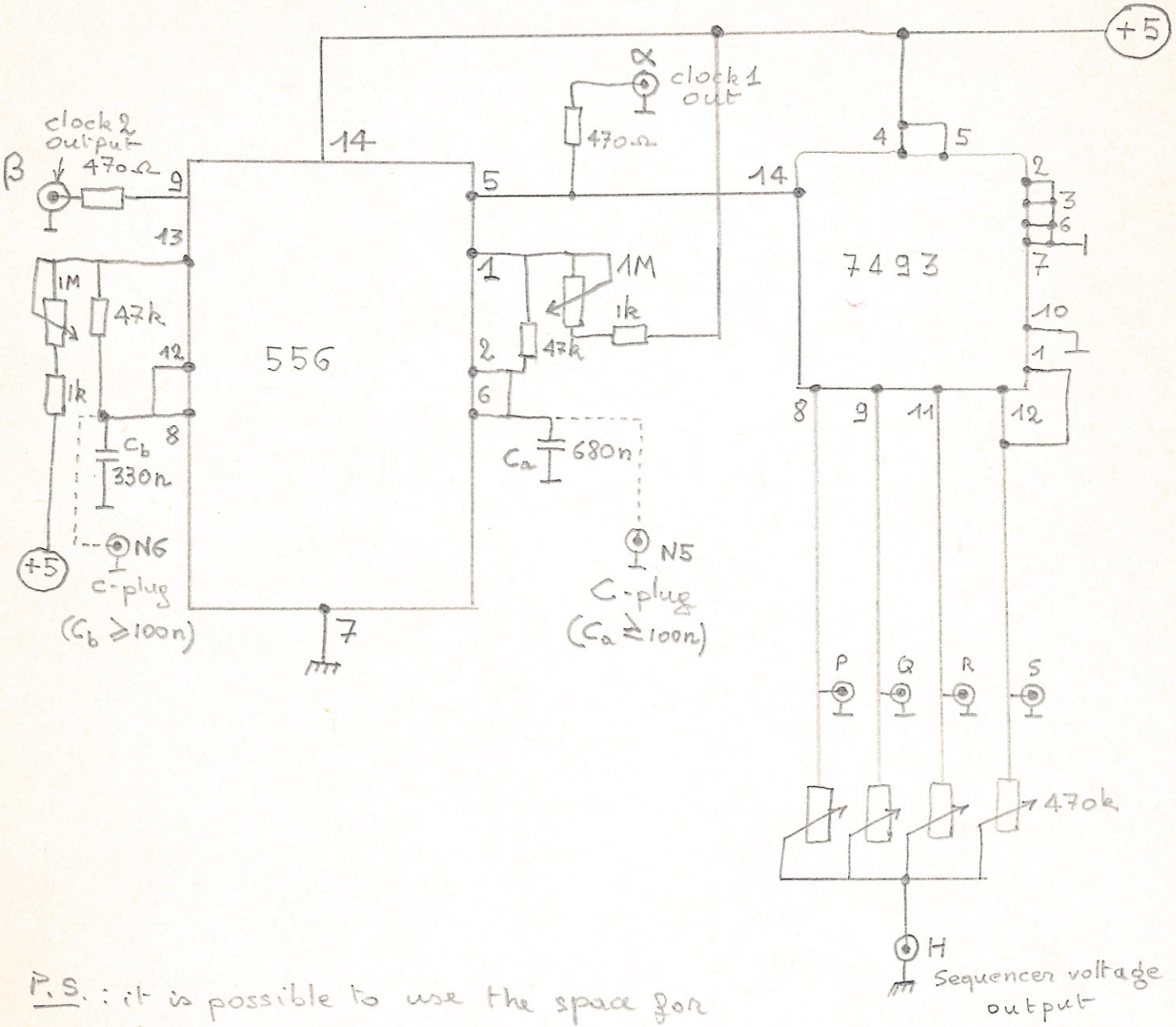
LOGIC - CONTROL



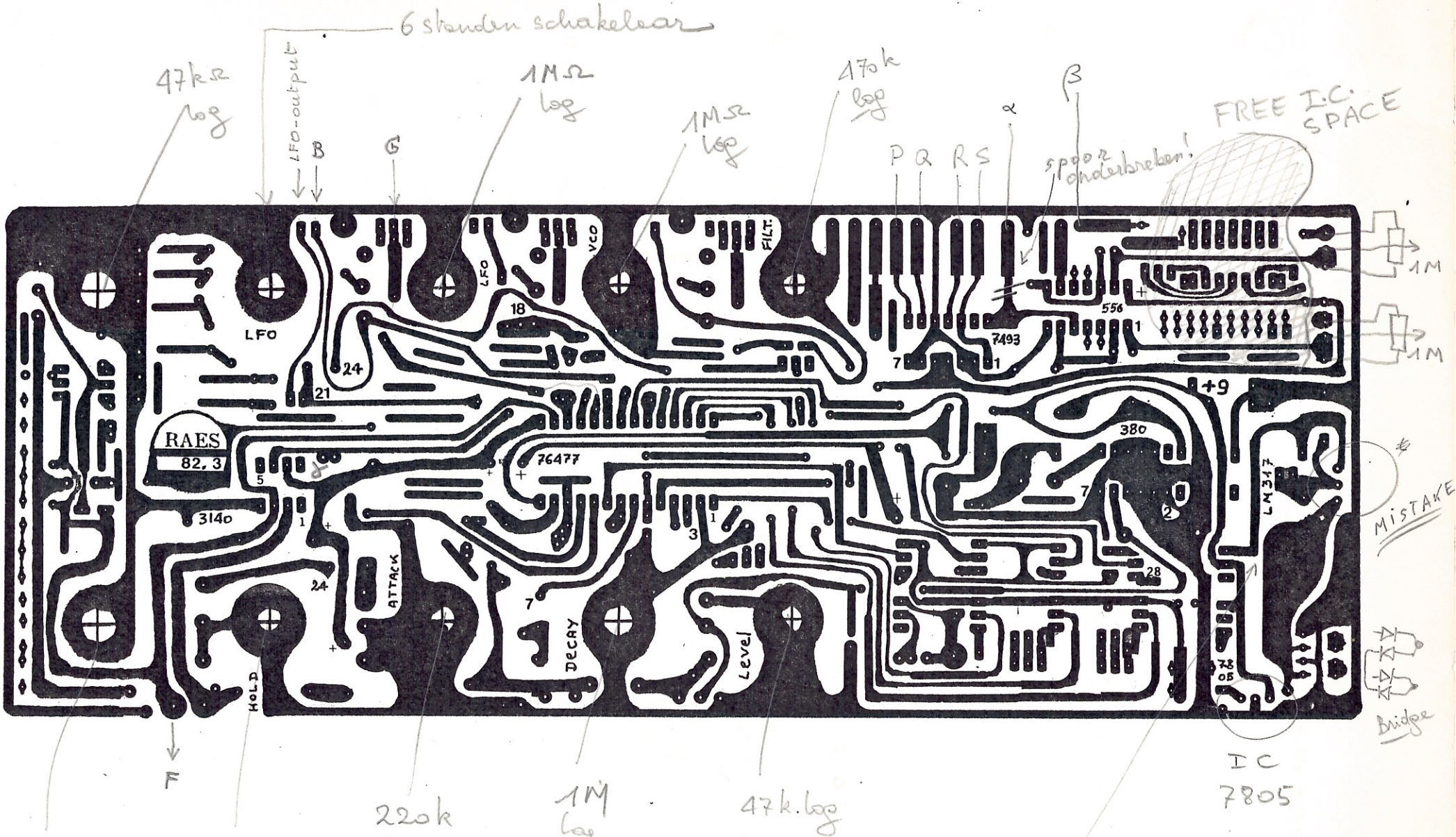
ONE SHOT & ENVELOPE



SEQUENCER



P.S. : it is possible to use the space for 1 I.C. to make a second BCD Sequencer. Use of 7490 chip results in different patterns.



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B-9000 Gent
tel. 091-23.80.89

SYNTHELOG III

ONE SHOT TIME

C = 10µ 26ms < Δt < 3,7s potm: 470k

ATTACK TIME

C = 3µ3 10 ms < Δt < 0,66s potm: 220k

DECAY TIME

C = 3µ3 10 ms < Δt < 3,3s potm: 1M

LFO

potm: 1M

Range 1	500pF	370kHz > f >	1280 Hz
2	1n	193kHz > f >	640 Hz
3	10n	19,3 Hz > f >	64 Hz
4	100n	1,93 Hz > f >	6,4 Hz
5	1µ	193 Hz > f >	0,64 Hz
6	10µ	19,3 Hz > f >	0,064 Hz

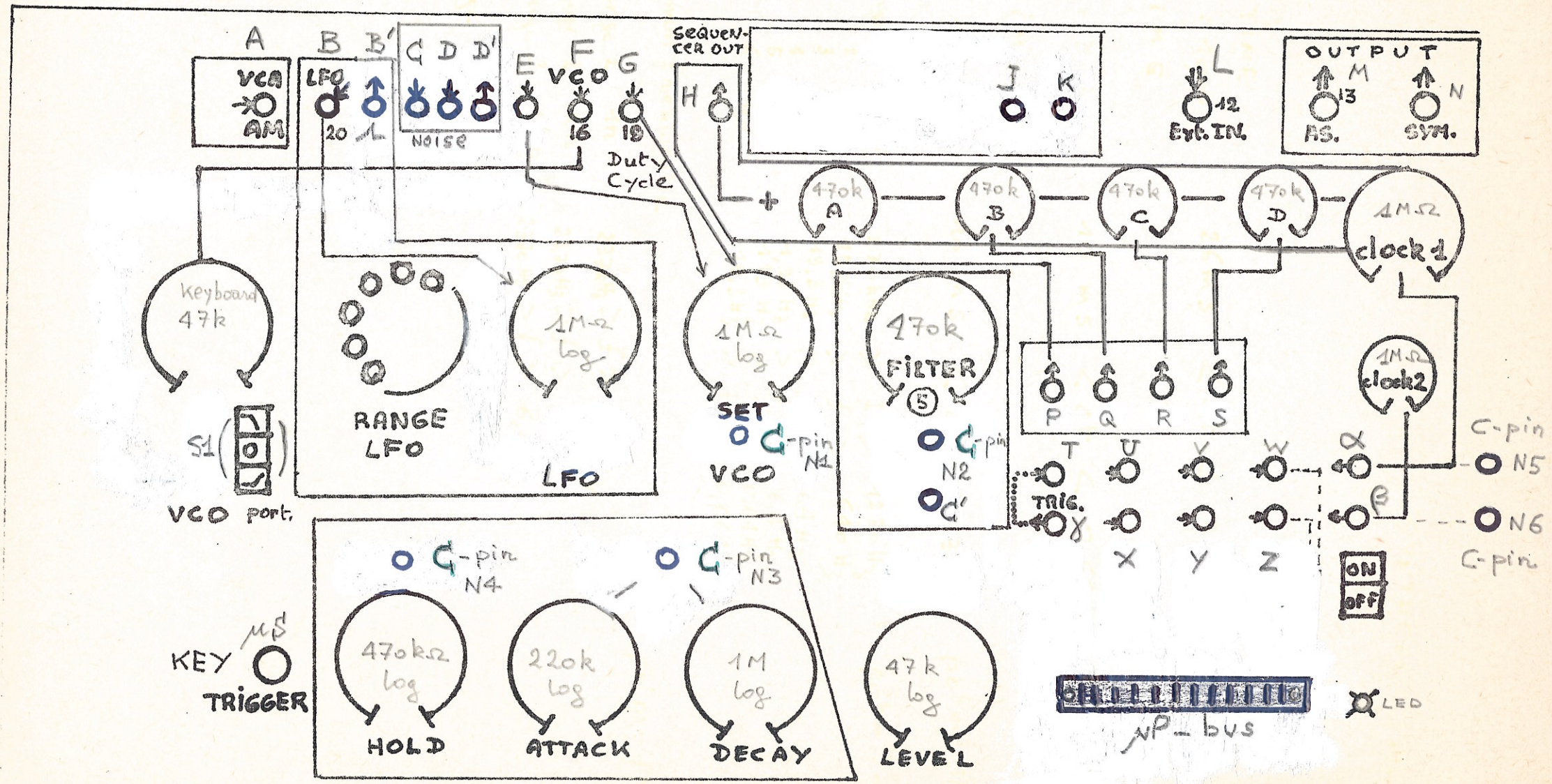
VCO - minimum frekwentie

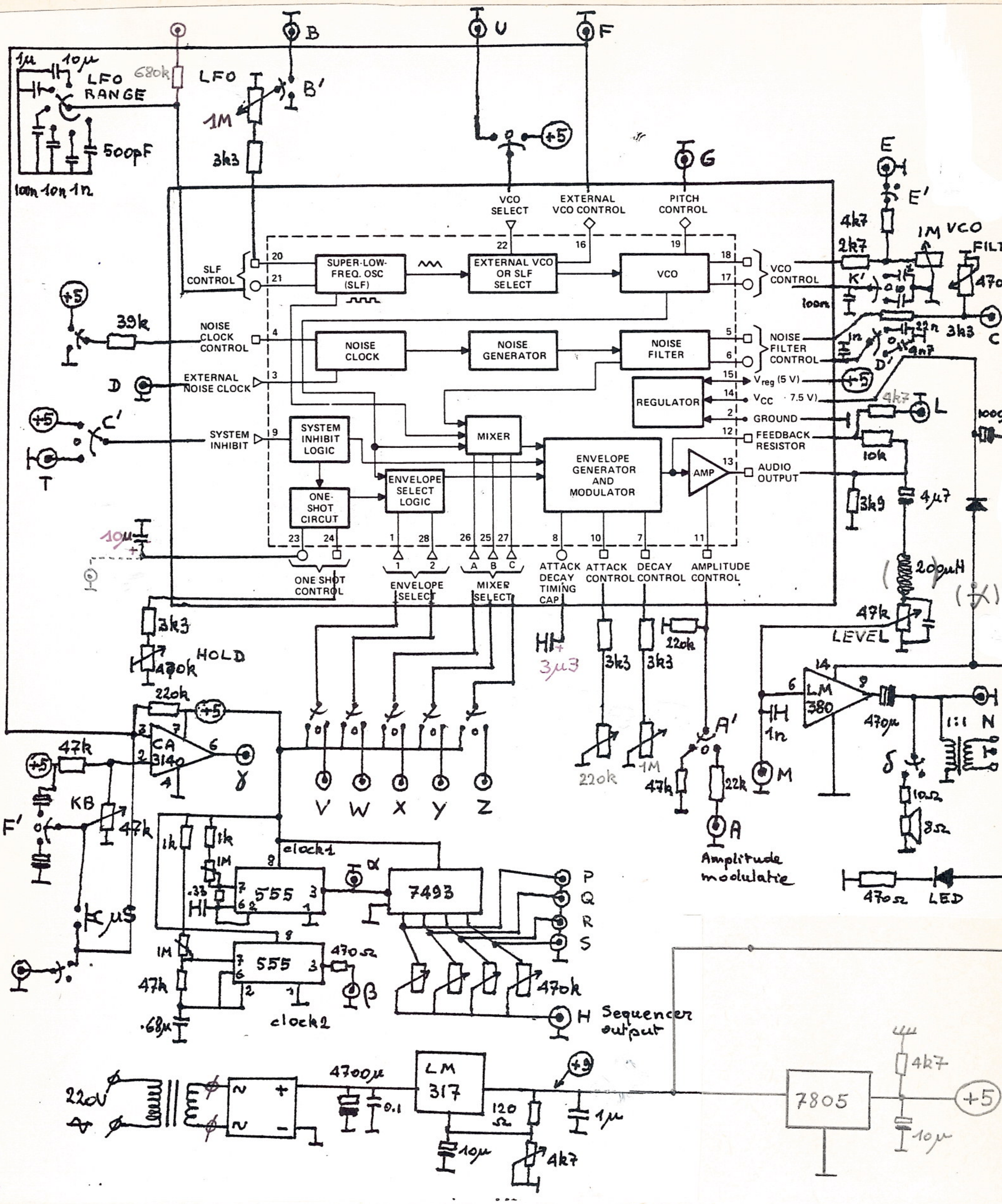
potm: 1M

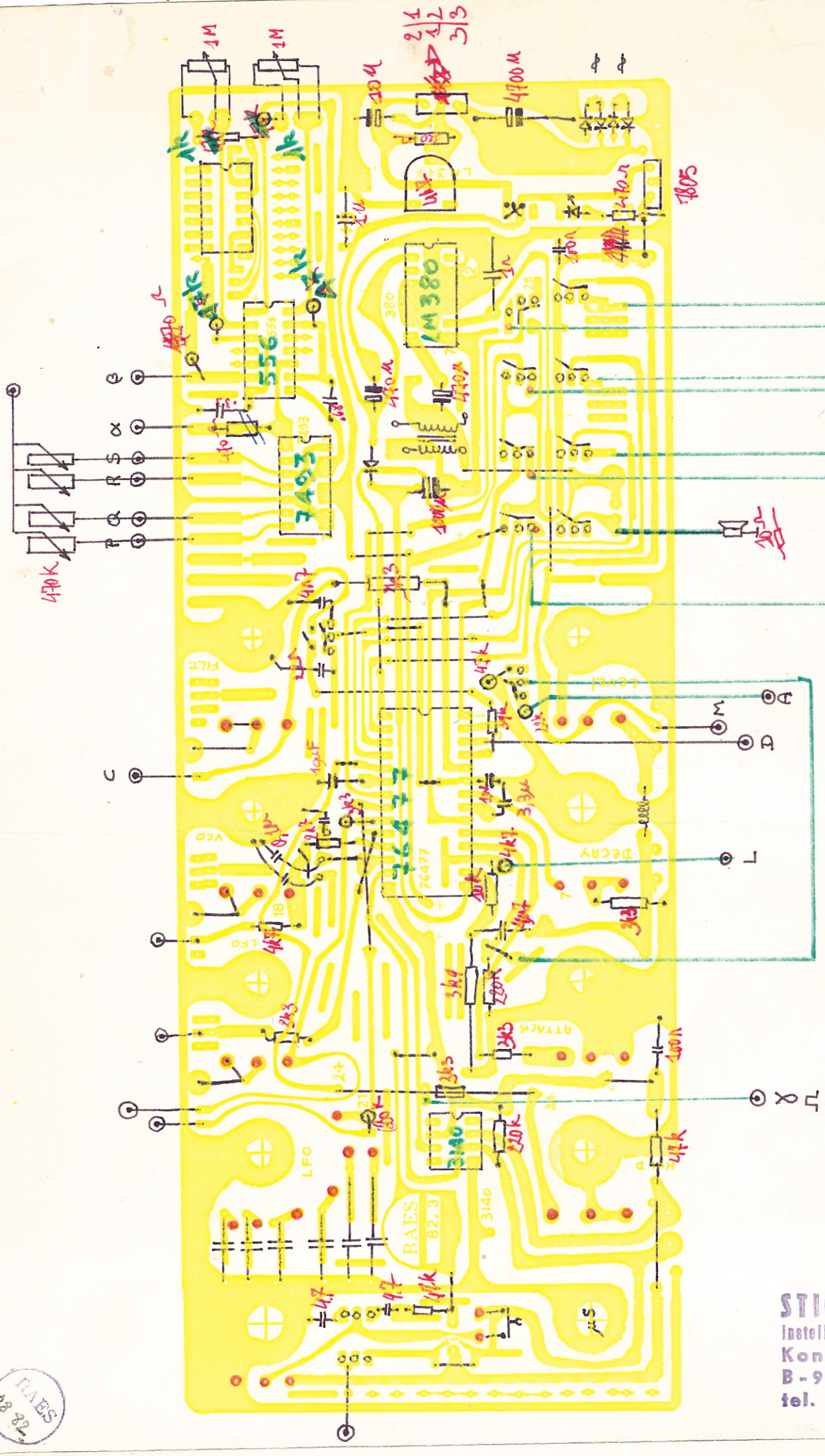
Range 1	1n	237kHz > f > 640 Hz
Range 2	10n	23,7kHz > f > 64 Hz
Range 3	100n	2370 Hz > f > 6,4 Hz

V.C. range ratio: 1:10

SYNTHELOG III




LFO RANGE
680k
LFO
1M
3k3
500pF
100n 10n 1n
VCO SELECT
EXTERNAL VCO CONTROL
PITCH CONTROL
SLF CONTROL
SUPER-LOW-FREQ. OSC (SLF)
EXTERNAL VCO OR SLF SELECT
VCO
VCO CONTROL
NOISE CLOCK CONTROL
NOISE CLOCK
NOISE GENERATOR
NOISE FILTER
NOISE FILTER CONTROL
EXTERNAL NOISE CLOCK
REGULATOR
GROUND
SYSTEM INHIBIT
SYSTEM INHIBIT LOGIC
MIXER
FEEDBACK RESISTOR
ENVELOPE GENERATOR AND MODULATOR
AMP
AUDIO OUTPUT
ONE-SHOT CIRCUT
ENVELOPE SELECT LOGIC
ONE SHOT CONTROL
ENVELOPE SELECT
MIXER SELECT
ATTACK DECAY TIMING CAP
ATTACK CONTROL
DECAY CONTROL
AMPLITUDE CONTROL
39k
4k7
2k7
1M VCO
3k3
10k
3k9
4μ7
200μH
47k LEVEL
HOLD
470k
220k
CA 3140
47k
KB
LM 380
470μ
Amplitude modulatie
555
7493
clock1
clock2
Sequencer output
470Ω
LED
LM 317
4700μ
120 Ω
7805
220V



Synthelog III

82.3.

print layout

&

films

S Y N T H E L O G III Type 82.9

Bouwinstructies

Gebruikte I.C.'s :

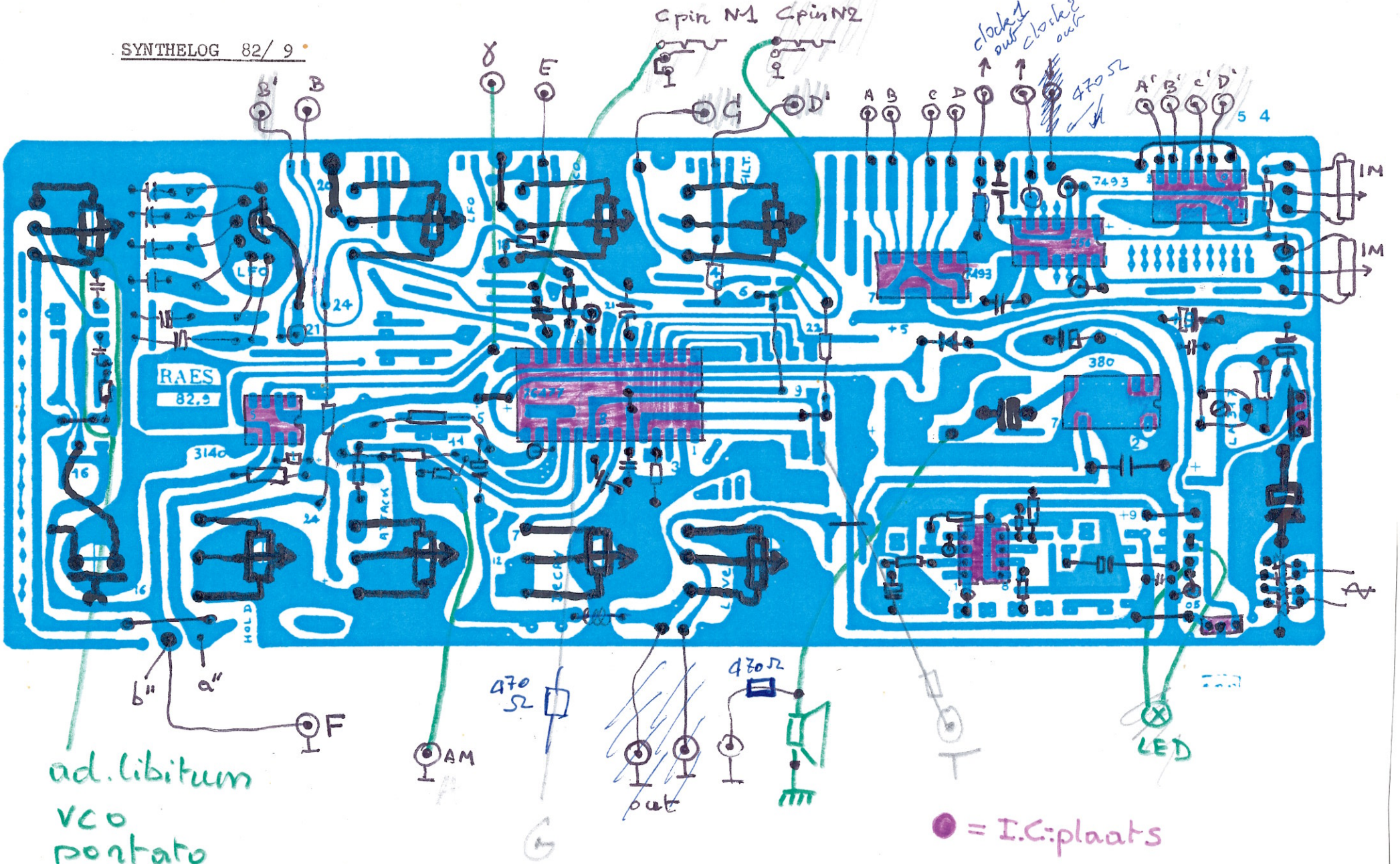
SN 76477
LM 317
7805
556
7493
7493
CA 3140
LF 353
LM 380

Diodes :

5 stuks 1N4007

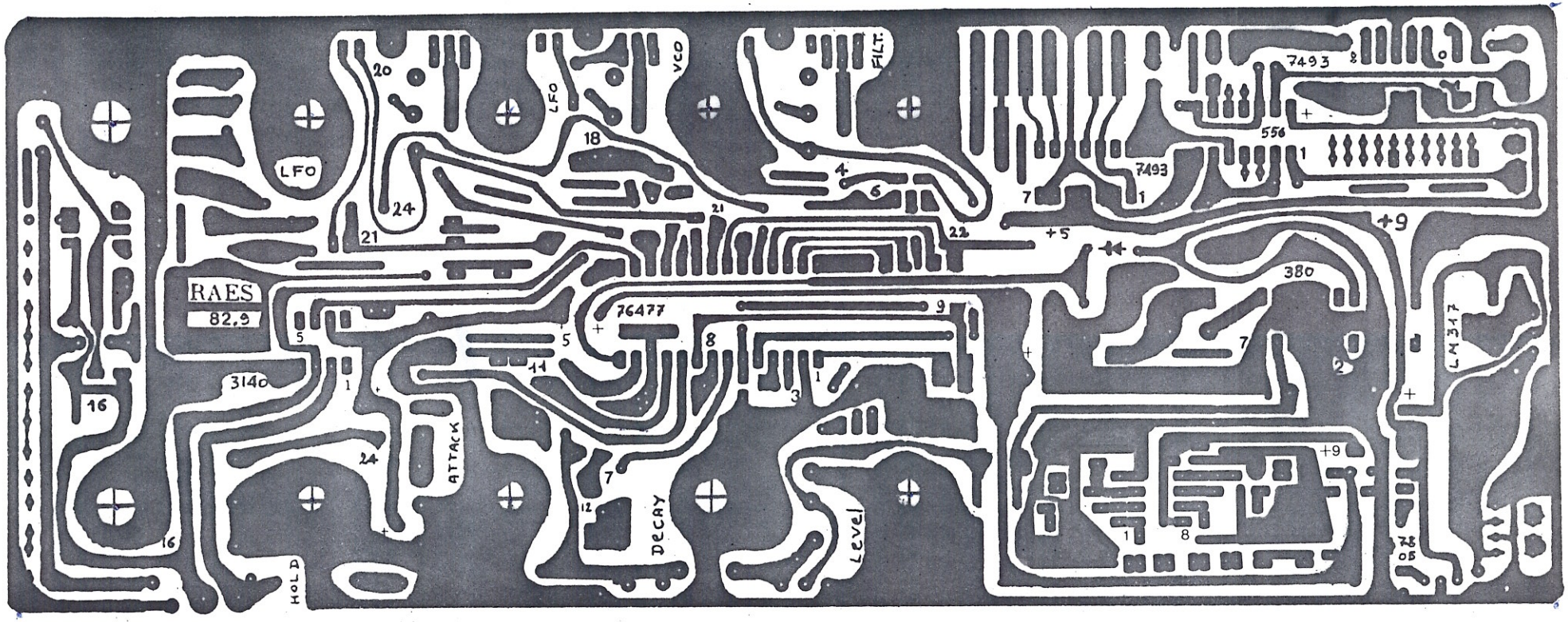
Potmeters:

1 M ohm	vco log.
1 M ohm	lfo log.
470 k ohm	filt.log.
47 k ohm	volume , log.
47 k ohm	vco-preset KB. log
4,7k ohm	trimpot voeding
220kohm	attack log.
1 M ohm	decay log
470 k ohm	hold log
1 M ohm	clock log.
1 M ohm	clock 2 log.
4x 470kohm	sequencer 1 , log.
4x 470kohm	sequencer 2 , log.
ad. lib.:	
100kohm	reverb send
10 k	reverb return , log.



ad.libitum
vco
portato
S1

● = I.C.-plaats


LFO
20
LFO
VCO
FILT
18
4
6
24
21
21
22
RAES
82,9
5
5
76477
9
8
11
3140
1
1
3
16
ATTACK
24
7
12
DECAY
Level
16
HOLD
7493
556
7493
1
7
+5
14
+9
380
7
8
+9
8
LM317

S Y N T H E L O G III Type 82.9

Bouwinstructies

Gebruikte I.C.'s :

SN 76477
LM 317
7805
556
7493
7493
CA 3140
LF 353
LM 380

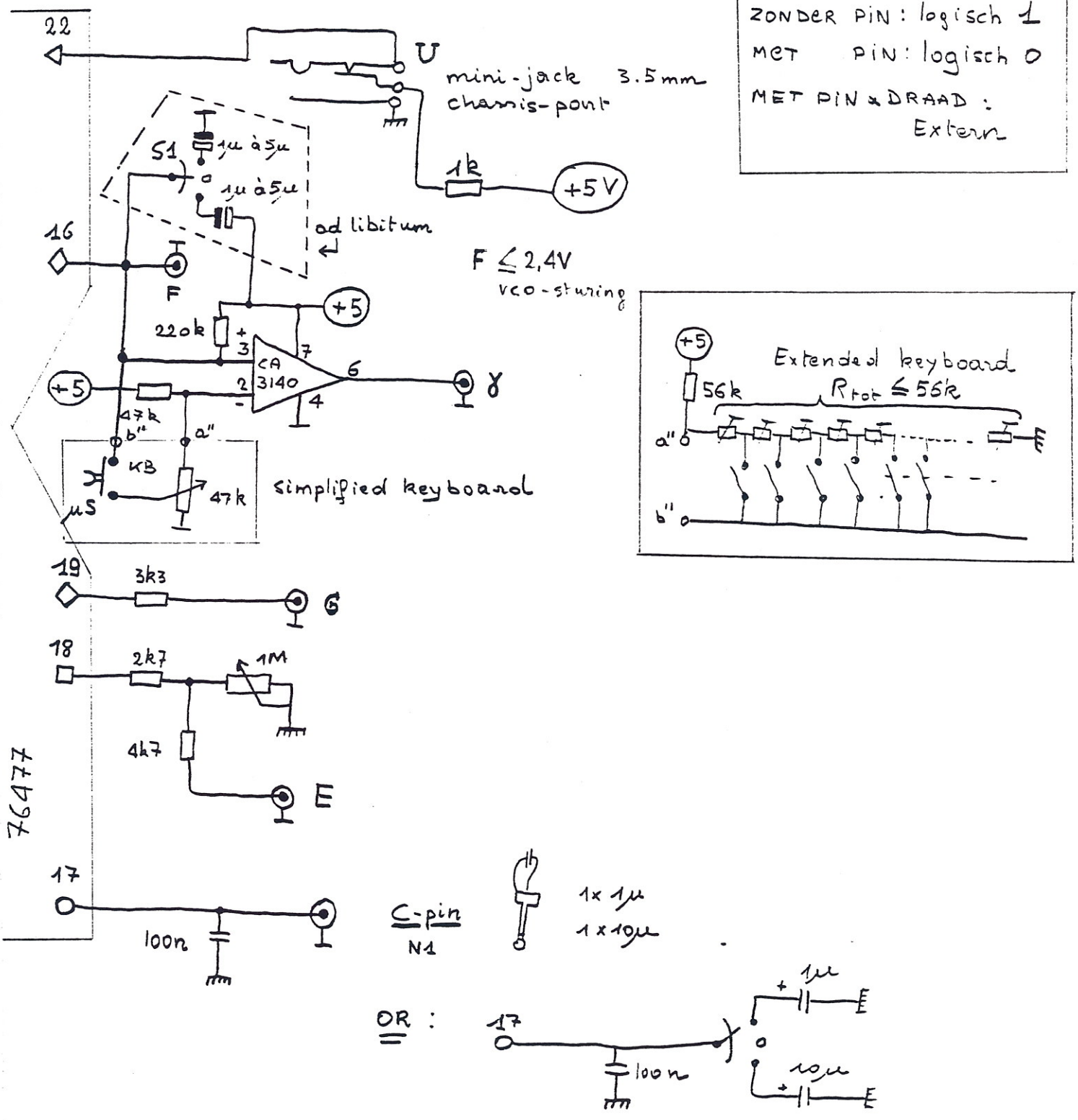
Diodes :

5 stuks 1N4007

Potmeters:

1 M ohm	vco log.
1 M ohm	lfo log.
470 k ohm	filt.log.
47 k ohm	volume , log.
47 k ohm	vco-preset KB. log
4,7k ohm	trimpot voeding
220kohm	attack log.
1 M ohm	decay log
470 k ohm	hold log
1 M ohm	clock log.
1 M ohm	clock 2 log.
4x 470kohm	sequencer 1 , log.
4x 470kohm	sequencer 2 , log.
ad. lib.:	
100ohm	reverb send
10 k	reverb return , log.

VCO



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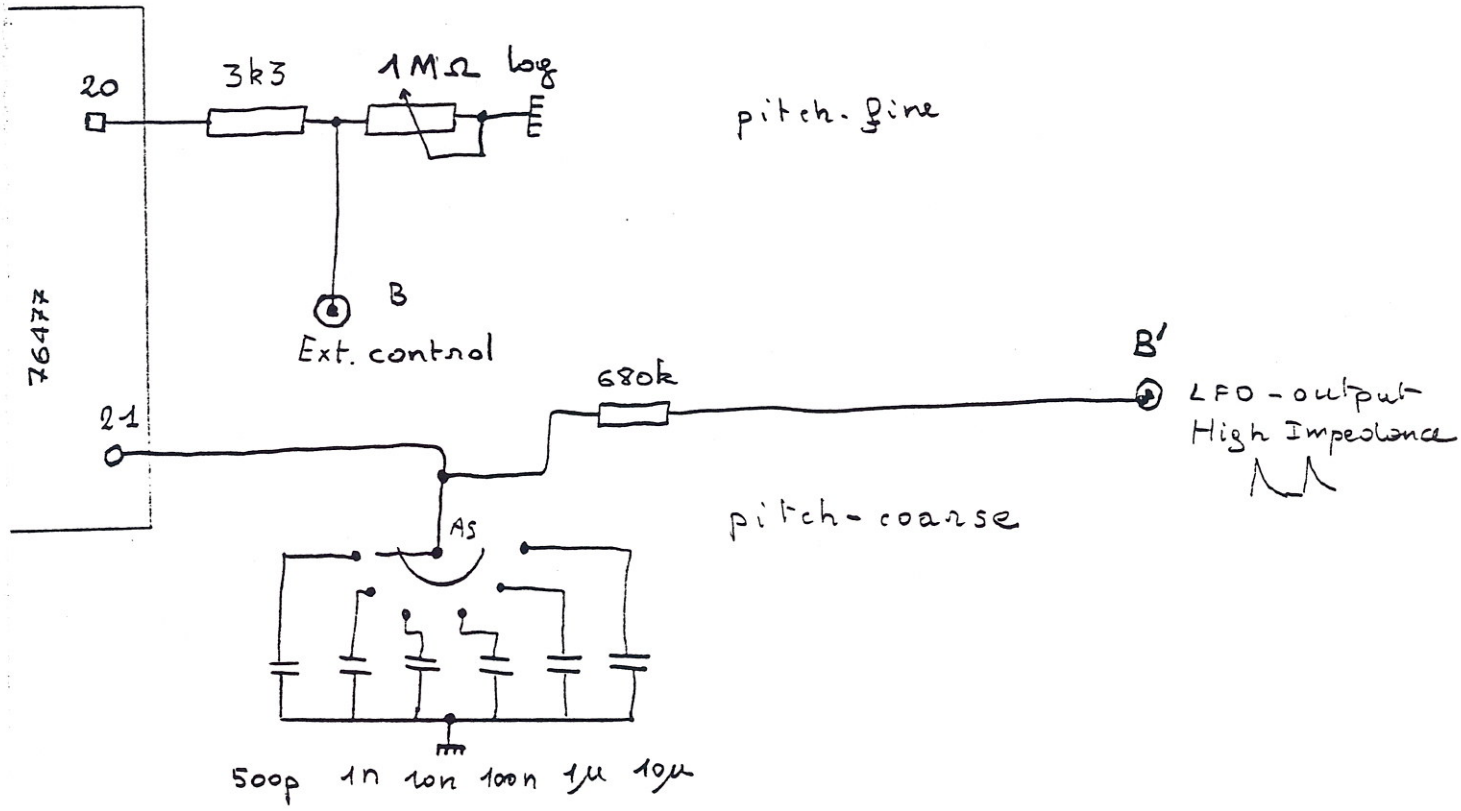
82.9

LFO



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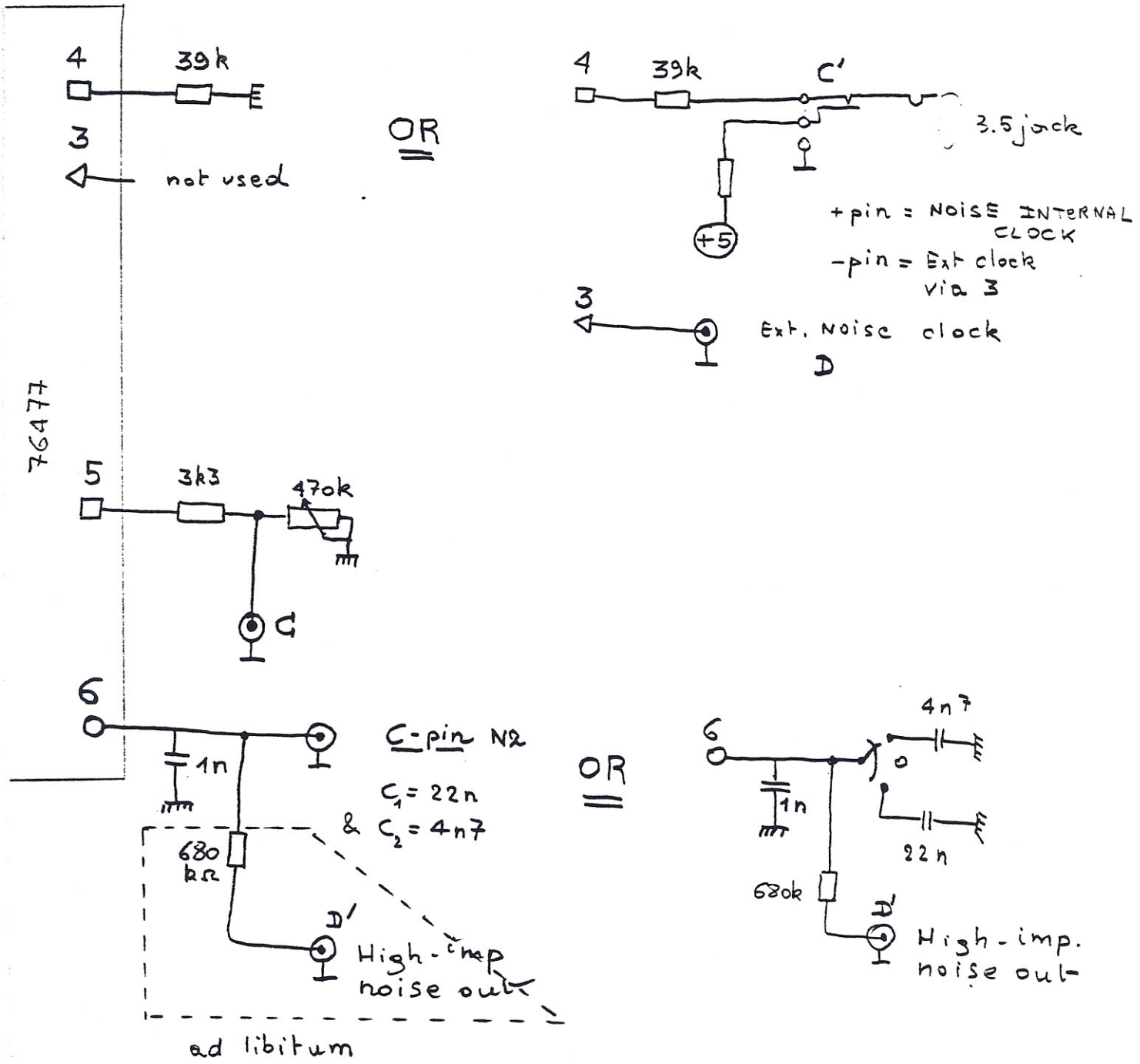
22.9

NOISE & FILTER



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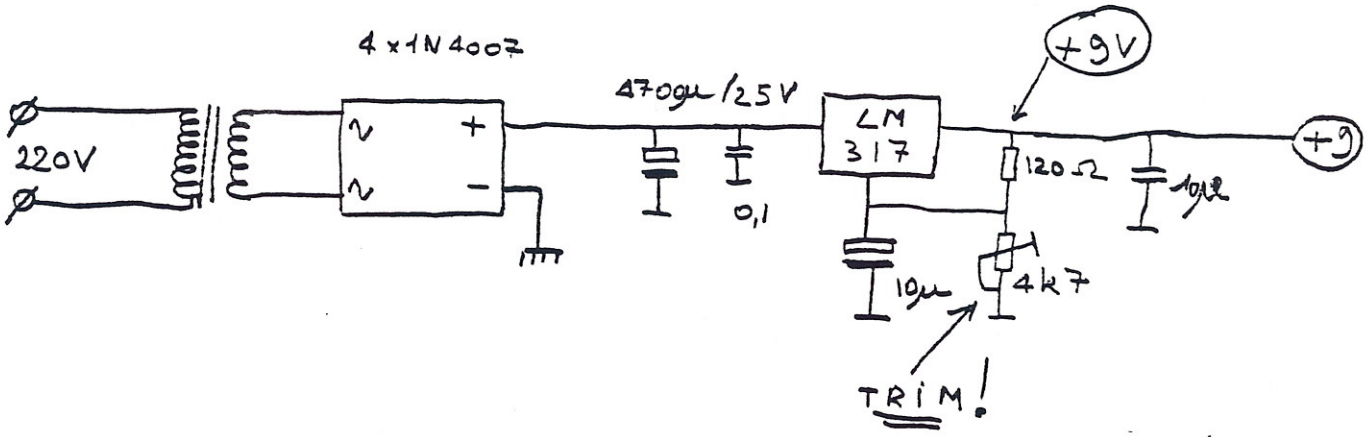
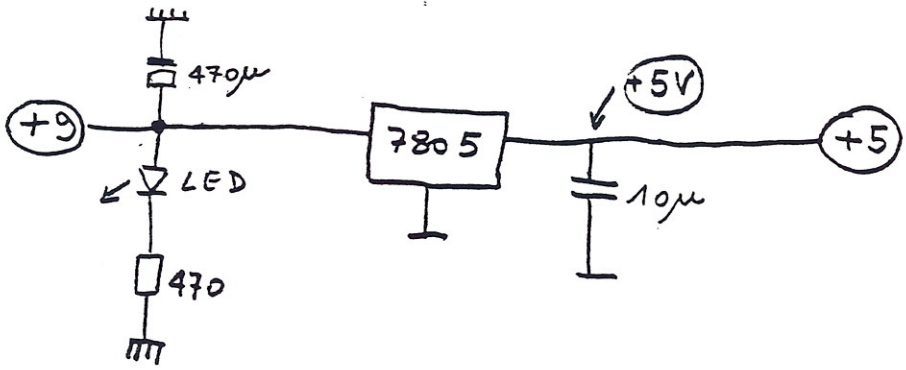
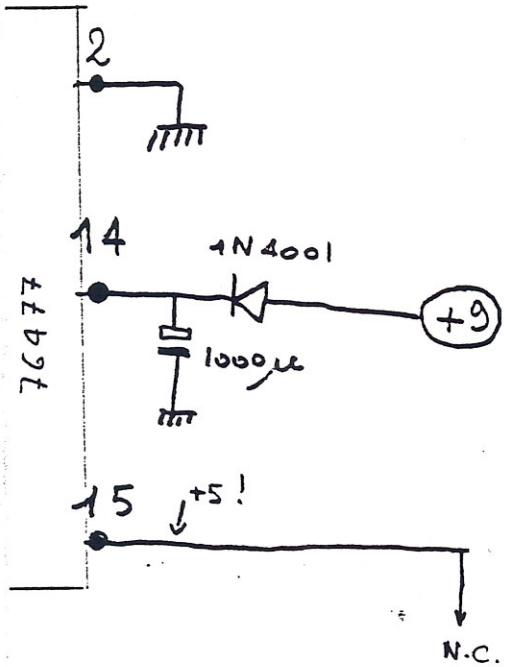
tel. 091-23.80.89

POWER SUPPLY







Controle : +5V ! internal power supply 76477.

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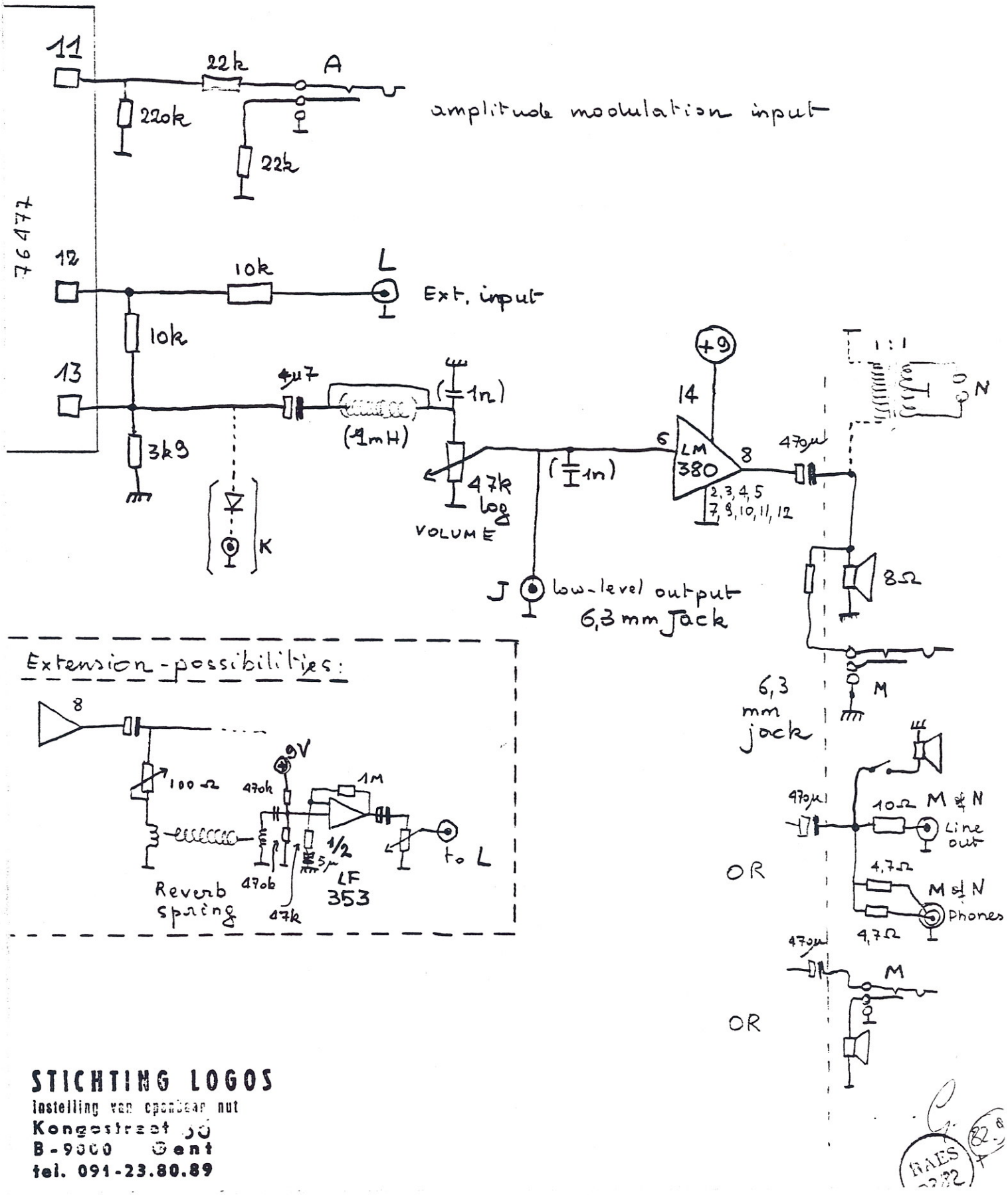
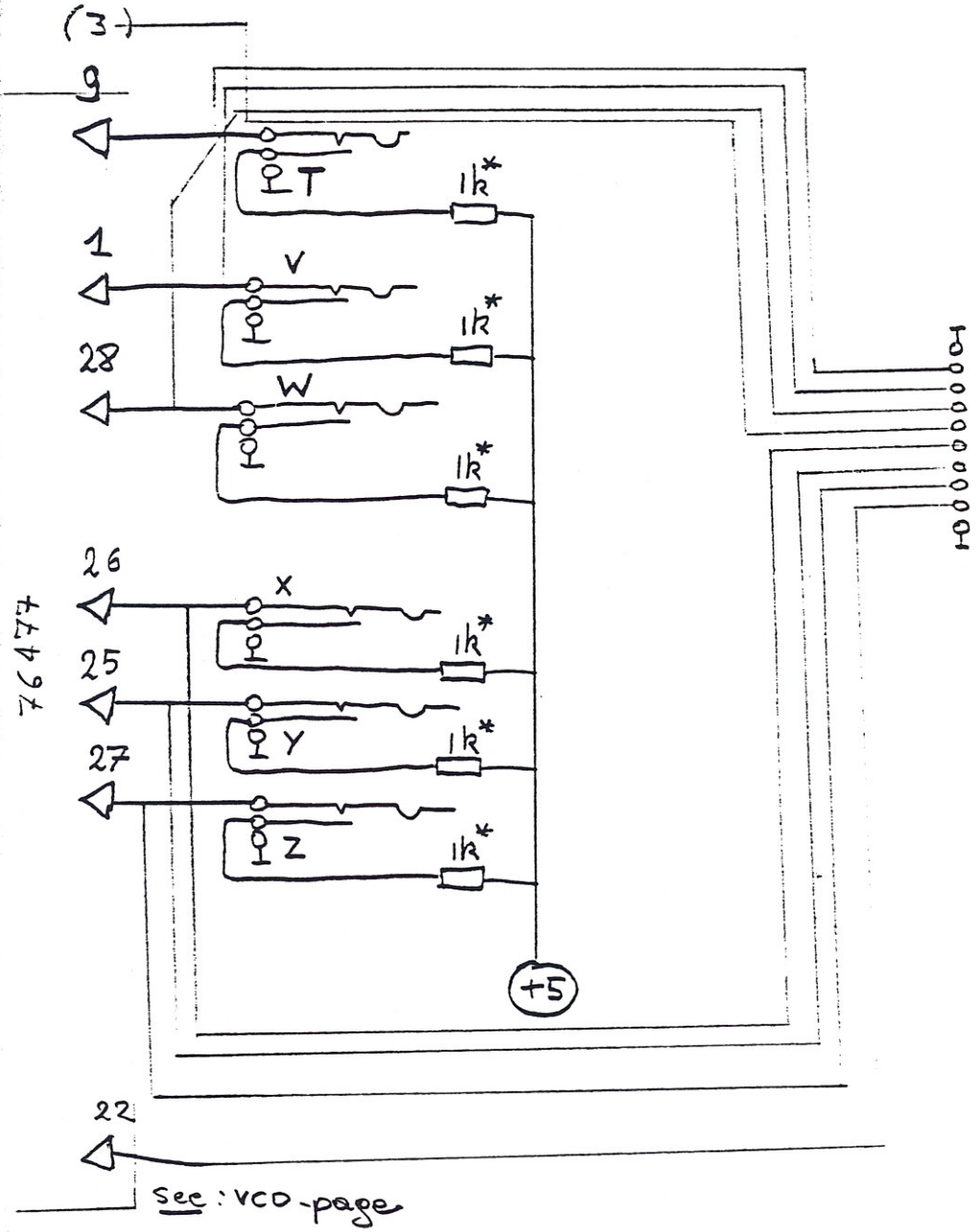
B-9000 Gent
tel. 091-23.80.89

OUTPUT OP-AMP /VCA



STICHTING LOGOS
Instelling van openbaar nut
Kongostraat 50
B-9000 Gent
tel. 091-23.80.89

LOGIC - CONTROL



* for µP interfacing, higher values may be required.
(OR) when µP is used, plugs should be inserted in the sockets.

STICHTING LOGOS
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Kongostraat 30
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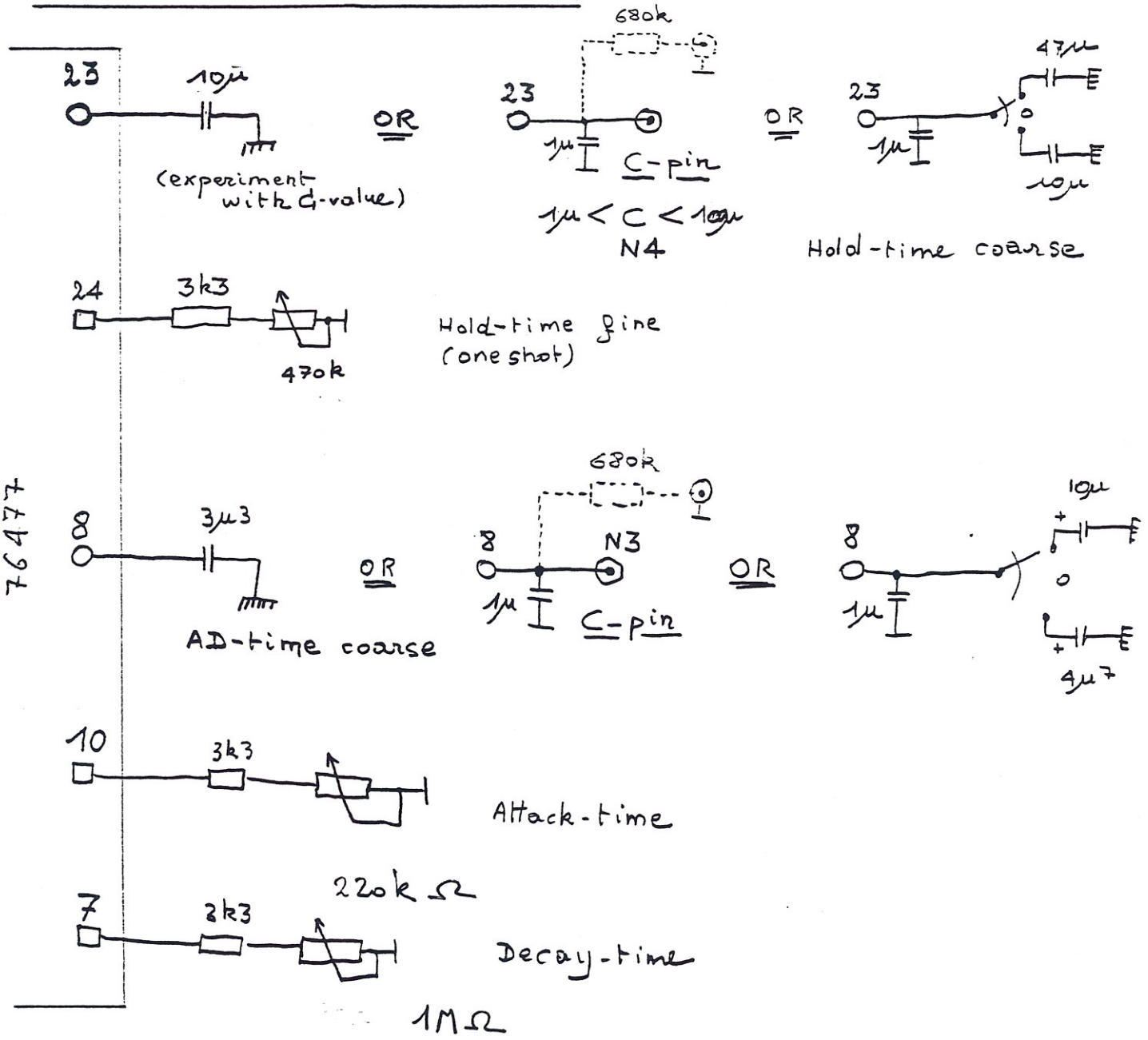
tel. 091-23.80.89

ONE SHOT & ENVELOPE



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Kongostraat 35
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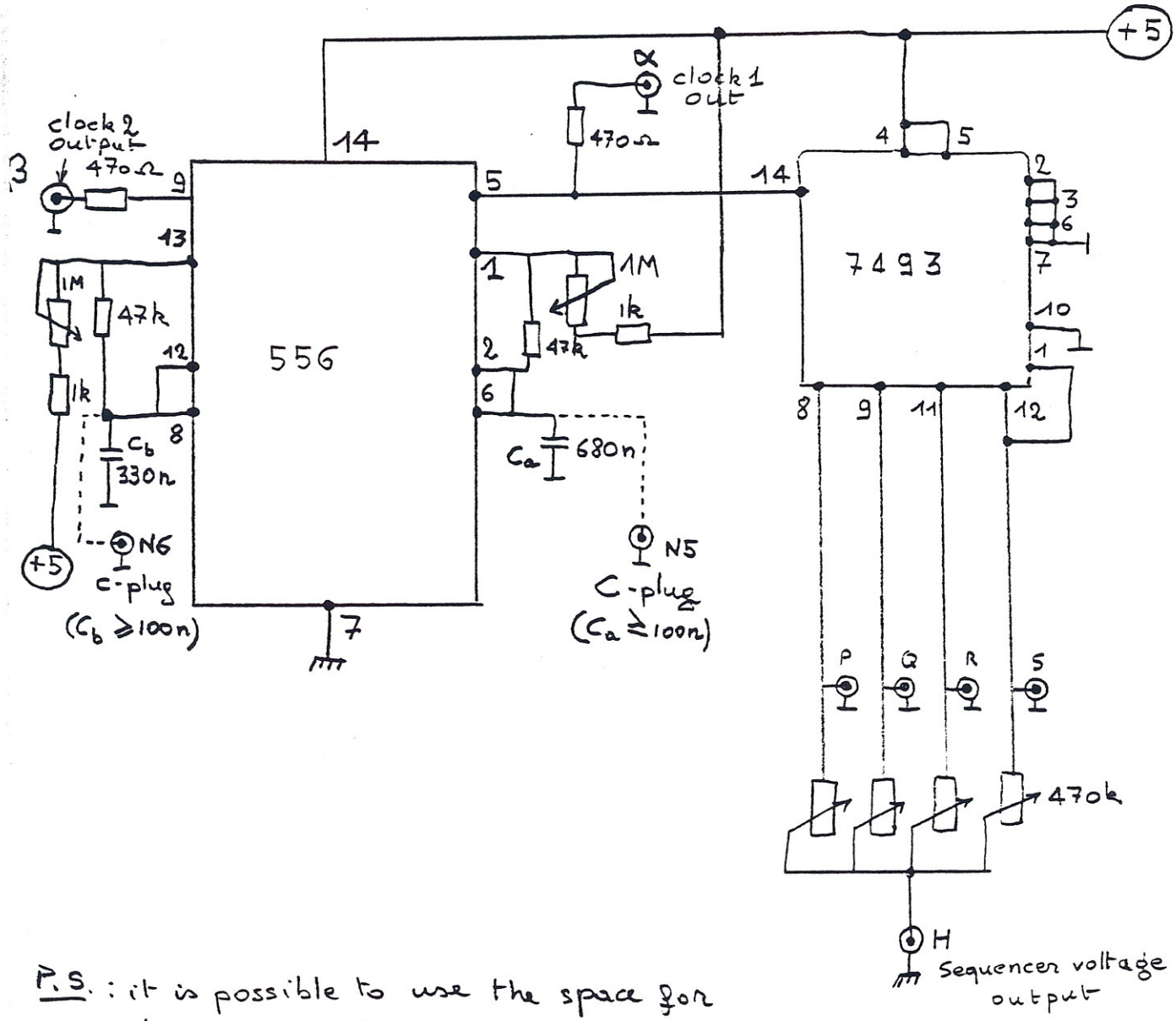
SEQUENCER



P.S. : it is possible to use the space for 1 I.C. to make a second BCD sequencer. Use of 7490 chip results in different patterns.

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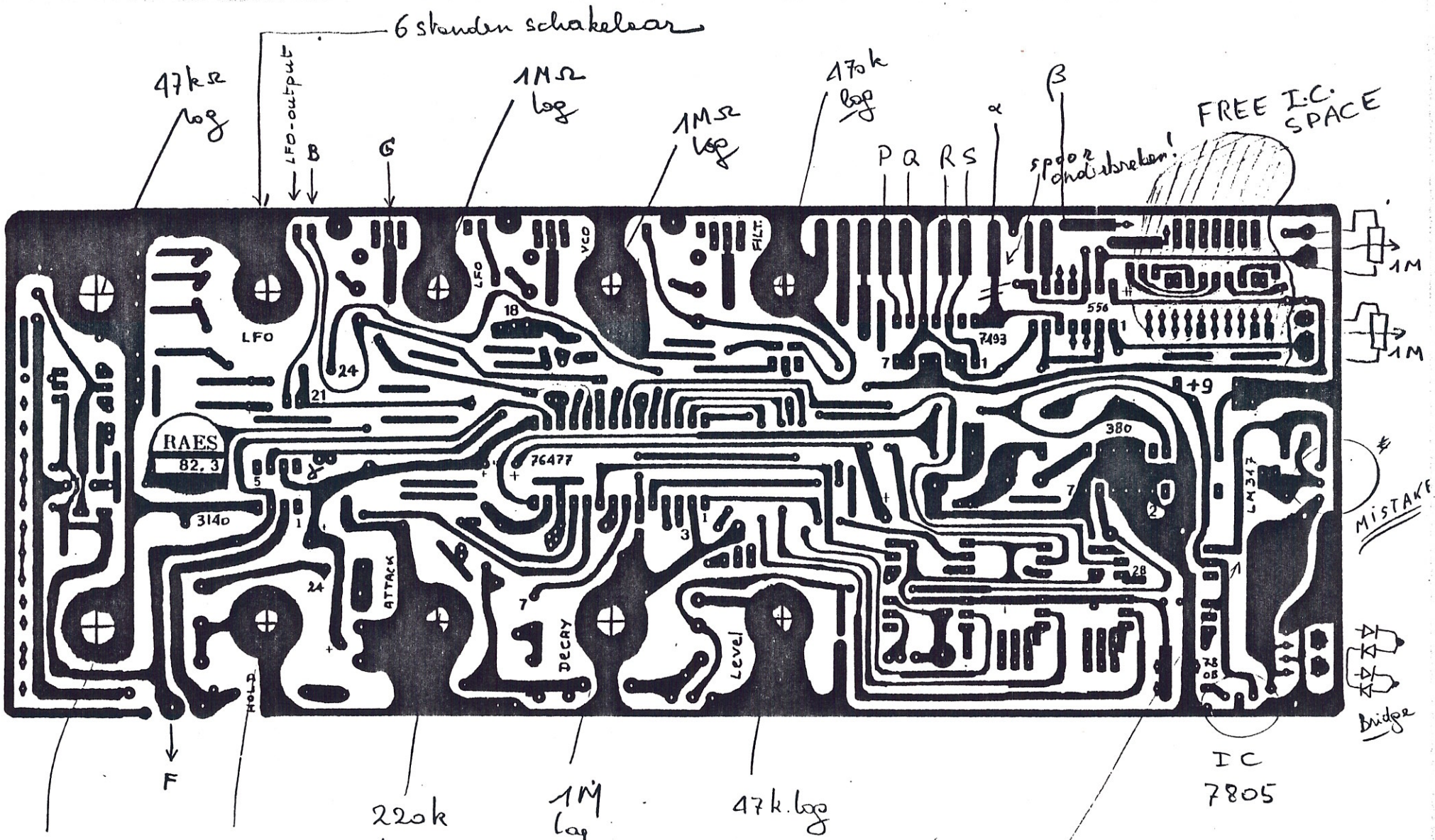

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B-9000 Gent
tel. 091-23.80.89

RAES OP 82 G

SYNTHELOG III

ONE SHOT TIME

C = 10µ 26ms < Δt < 3,7s potm: 470k

ATTACK TIME

C = 3µ3 10 ms < Δt < 0,66s potm: 220k

DECAY TIME

C = 3µ3 10 ms < Δt < 3,3s potm: 1M

LFO potm: 1M

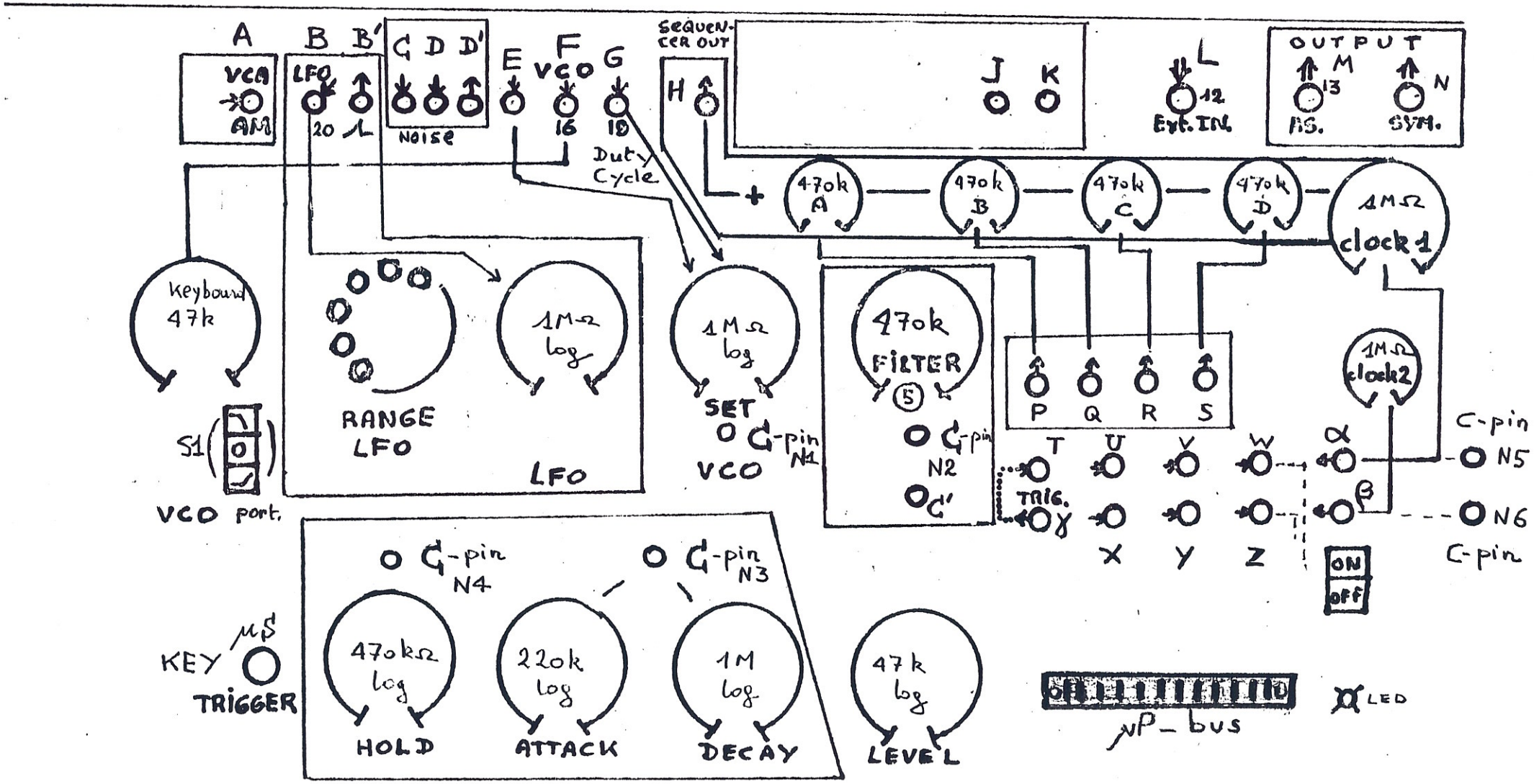
Range 1	500pF	370kHz > f >	1280 Hz
2	1n	193kHz > f >	640 Hz
3	10n	19,3 Hz > f >	64 Hz
4	100n	1,93 Hz > f >	6,4 Hz
5	1µ	193 Hz > f >	0,64 Hz
6	10µ	19,3 Hz > f >	0,064 Hz

VCO - minimum frekwentie potm: 1M

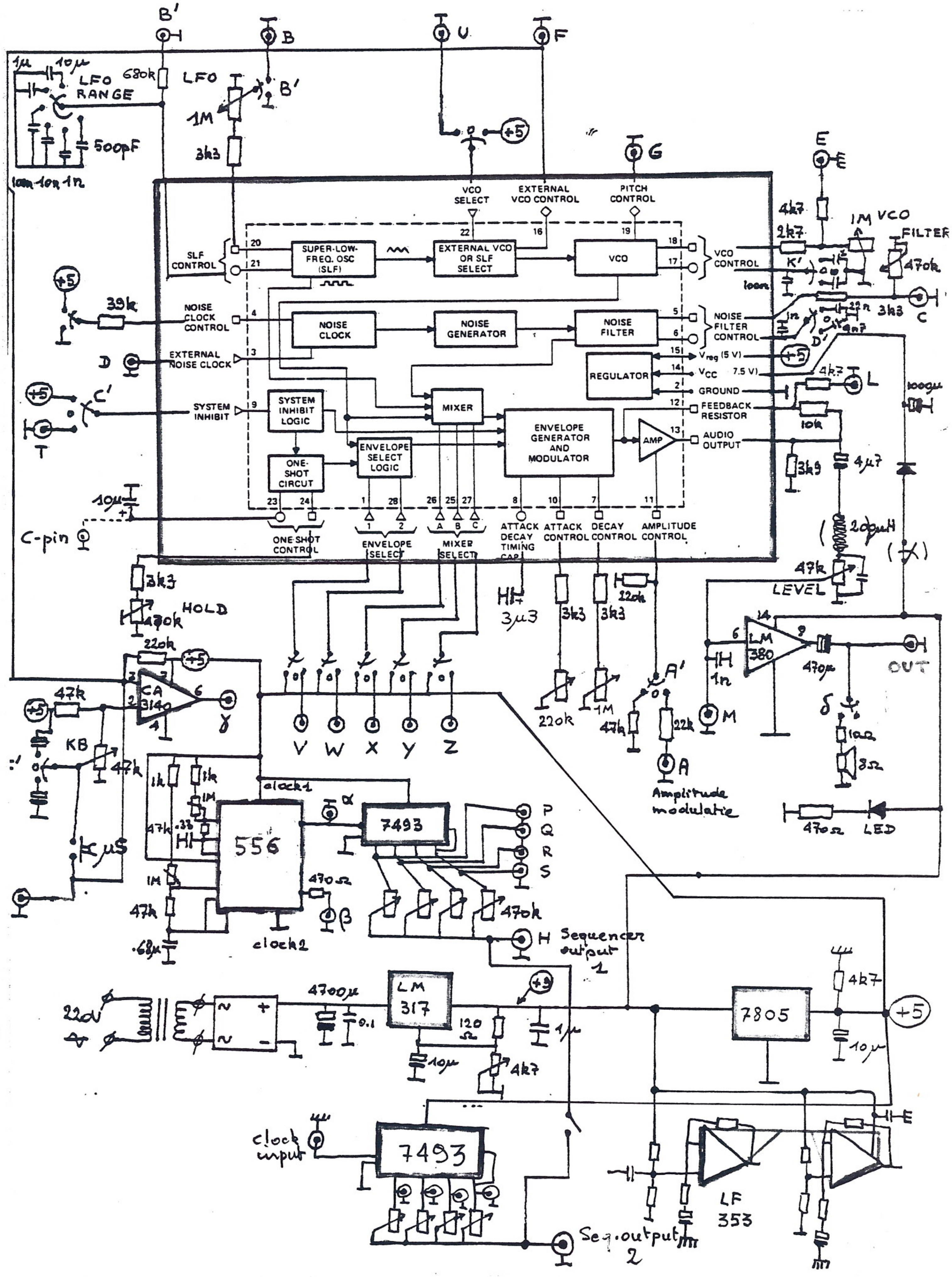
Range 1	1n	237kHz > f > 640 Hz
Range 2	10n	23,7kHz > f > 64 Hz
Range 3	100n	2370 Hz > f > 6,4 Hz

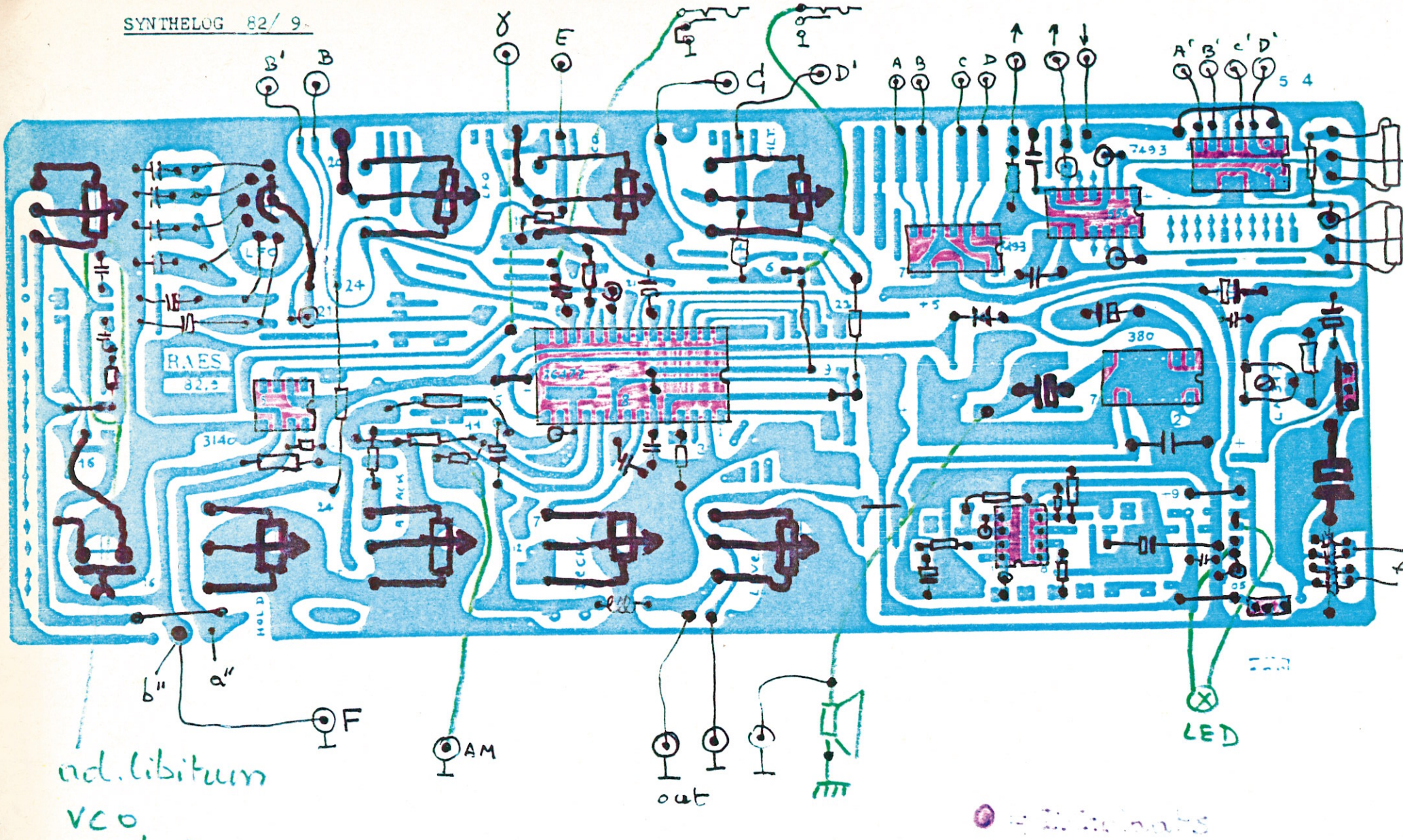
V.C. range ratio : 1:10

SYNTHELOG III

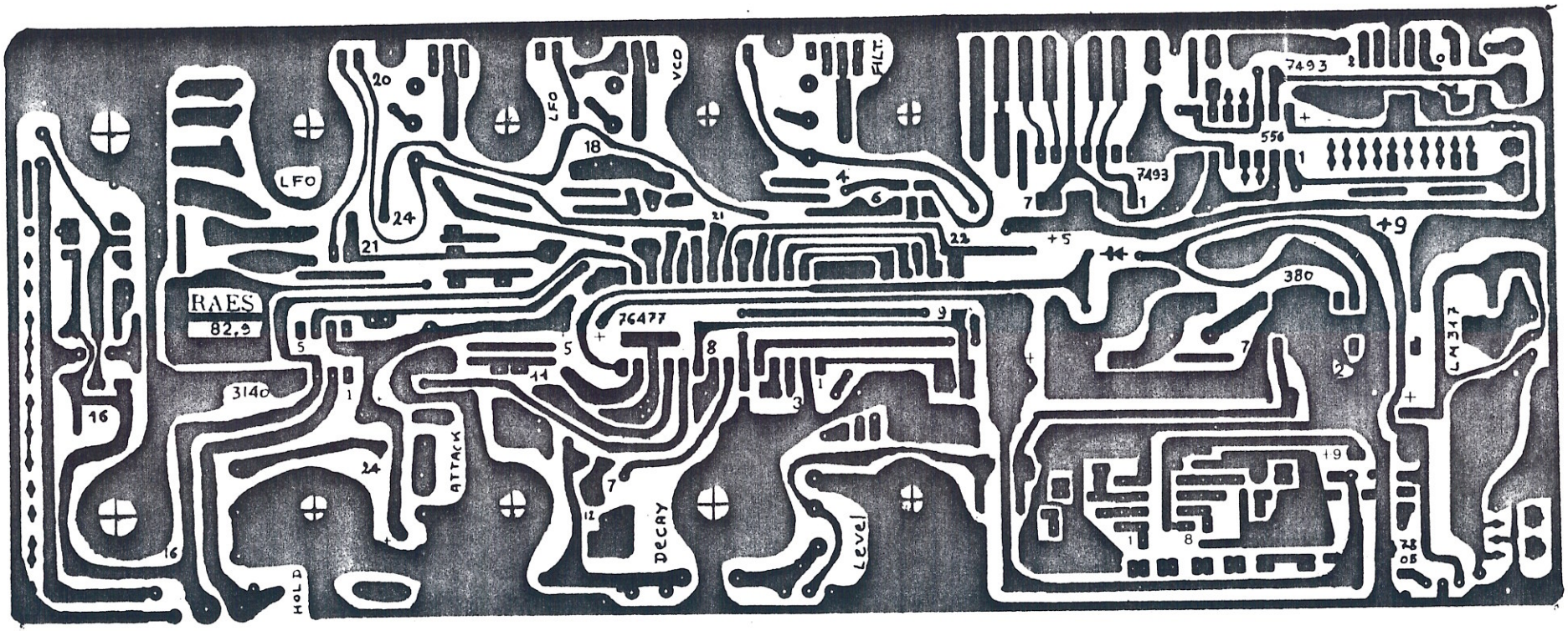


godfried-willem raes
muziekwetenschappen


B'
B
U
F
LFO RANGE
680k
LFO
1M
3k3
500pF
+5
G
E
VCO SELECT
EXTERNAL VCO CONTROL
PITCH CONTROL
SLF CONTROL
SUPER-LOW-FREQ. OSC (SLF)
EXTERNAL VCO OR SLF SELECT
VCO
VCO CONTROL
NOISE CLOCK CONTROL
NOISE CLOCK
NOISE GENERATOR
NOISE FILTER
NOISE FILTER CONTROL
EXTERNAL NOISE CLOCK
REGULATOR
Vreg (5 V)
VCC 7.5 V
GROUND
FEEDBACK RESISTOR
AUDIO OUTPUT
SYSTEM INHIBIT
SYSTEM INHIBIT LOGIC
MIXER
ENVELOPE GENERATOR AND MODULATOR
AMP
ONE-SHOT CIRCUIT
ENVELOPE SELECT LOGIC
ONE-SHOT CONTROL
ENVELOPE SELECT
MIXER SELECT
ATTACK DECAY TIMING CAP
ATTACK CONTROL
DECAY CONTROL
AMPLITUDE CONTROL
4k7
2k7
1M VCO
FILTER
470k
3k3
C
D
C'
T
L
39k
10k
3k9
4μ7
200μH
47k LEVEL
1000μ
C-pin
10μ
3k3
HOLD
470k
220k
CA 3140
γ
47k
KB
μS
3μ3
220k
1M
22k
A'
A
Amplitude modulatie
LM 380
470μ
OUT
M
1n
δ
10Ω
8Ω
470Ω
LED
V W X Y Z
clock1
556
α
7493
P Q R S
β
470Ω
470k
clock2
H Sequencer output 1
220V
4700μ
0.1
LM 317
+9
120Ω
1μ
10μ
4k7
7805
+5
clock input
7493
Seq. output 2
LF 353



nd. libitum
vco
pontato
S1


LFO
VCO
FILT
7493
556
7493
LFO
RAES
82.9
3140
76477
380
LM317
ATTACK
DECAY
Level
HOLD
+5
+9
+9

print

onderdelen op print.

(zonder jacks, knoppen, transfo, speaker

print + instructiepapieren & schema 800,-

IC's
- SN 76477
- CA 3140
- 7493
- 7490
- 556
- LF353 (ad libitum)
- LM380
- LM317
- 7805
- 5 x 1N4007

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13 potmeters.