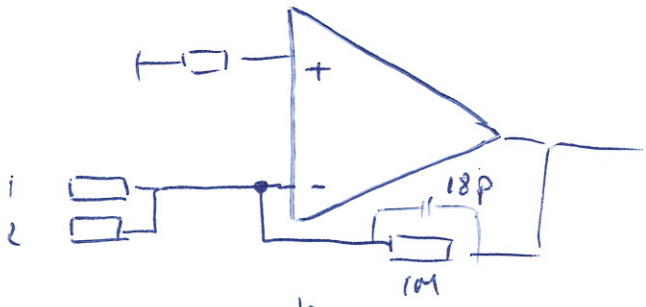
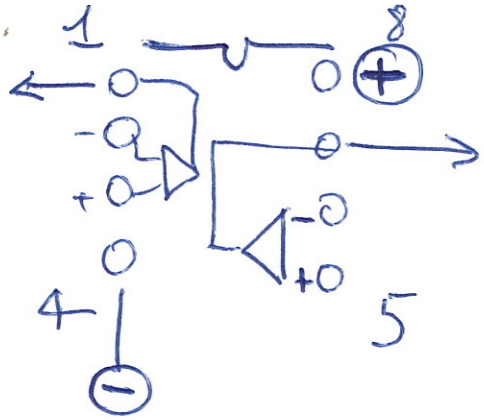
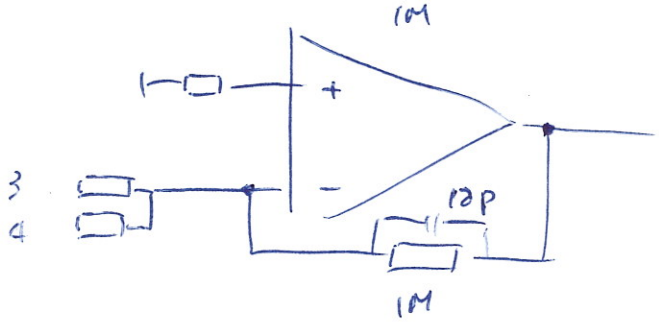
ATLANTA

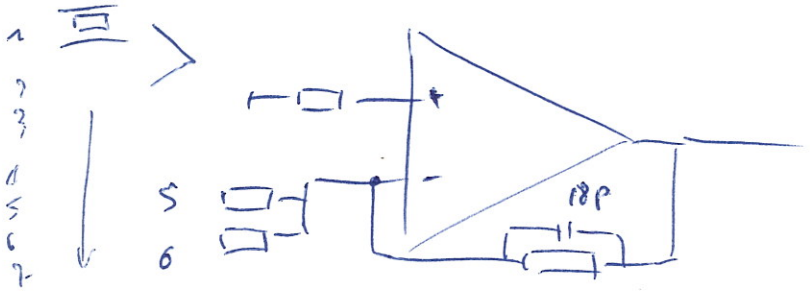
ALZICHT-SPECTRUM
DIN A4

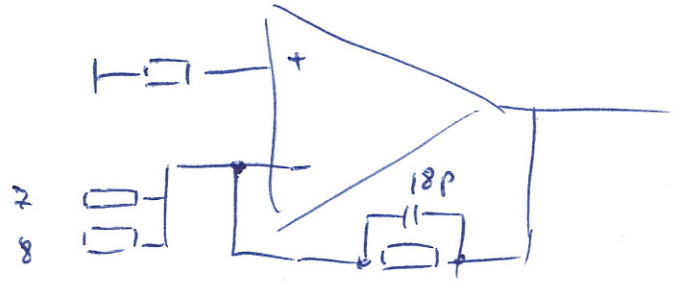
Mengtafel
met modulo-N oelers
voor Holosound

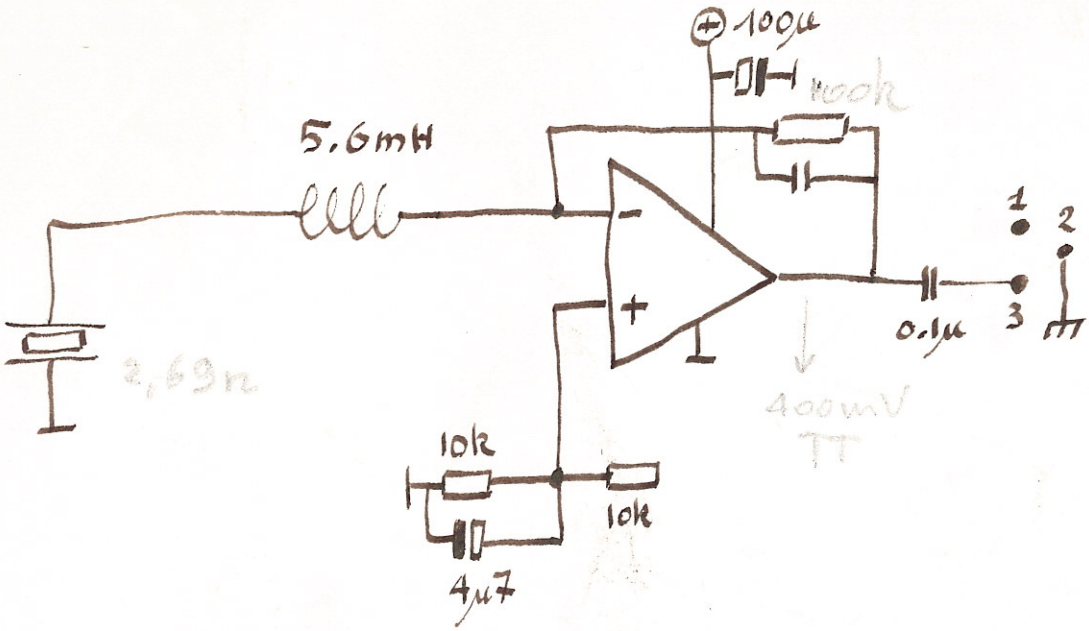

+
-
18p
1M


1
8
4
5


+
-
18p
1M


+
-
18p


+
-
18p


100µ
100k
5.6mH
1
2
3
0.1µ
2,69n
400mV
TT
10k
10k
4µ7

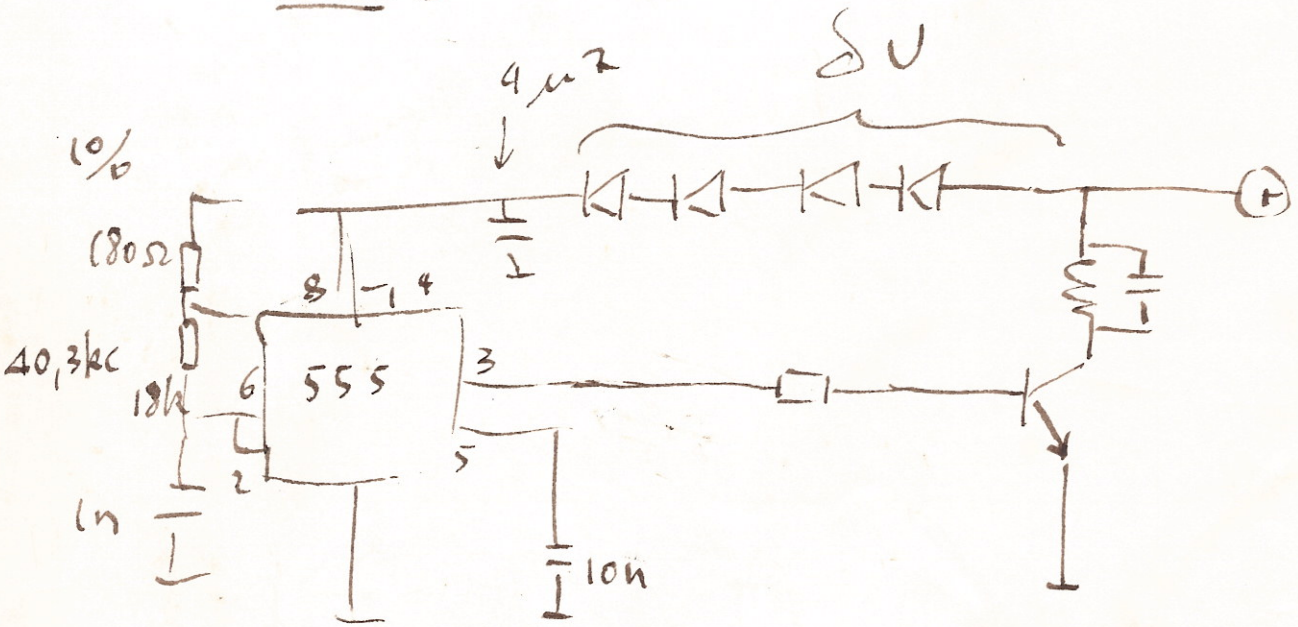
TIP 31B

$$f = \frac{1}{2\pi\sqrt{LC}}$$

PNP : TIP 32B

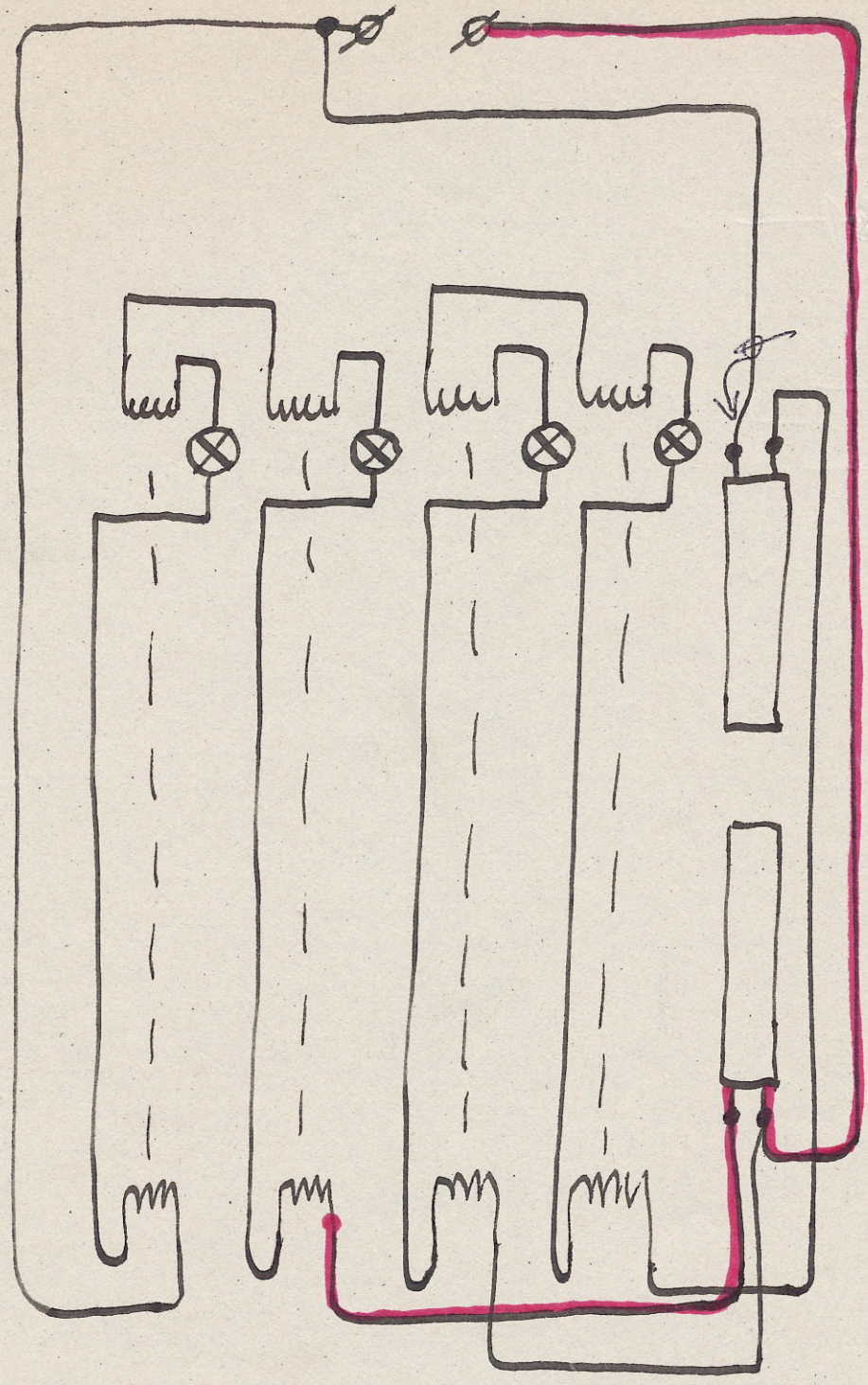
$$f^2 = \frac{1}{(2\pi)^2 \; 15.10^{-3} \; 15.10^{-9}}$$

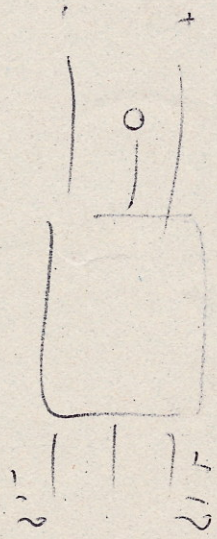
$$\Rightarrow f = \underline{10\,kHz}$$

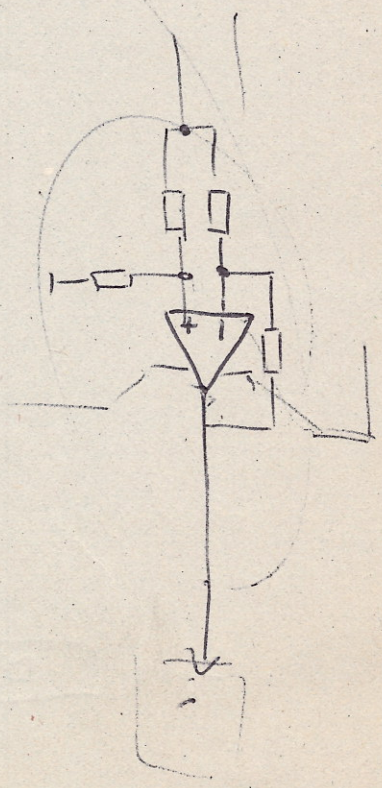


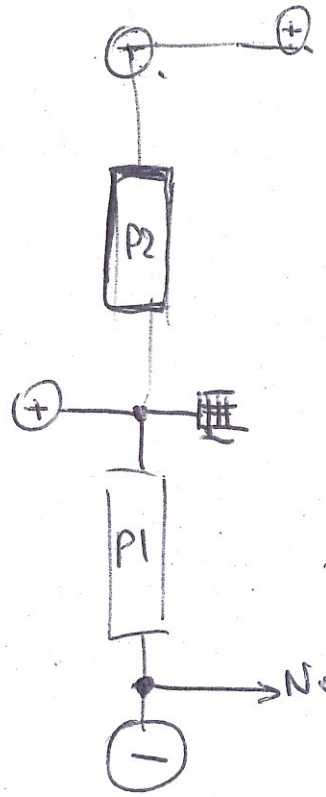
$$\left.\begin{array}{l} L = 4m7 \\ C_{tr.} = 2n5 \end{array}\right\} = \underline{46}\ kHz.$$

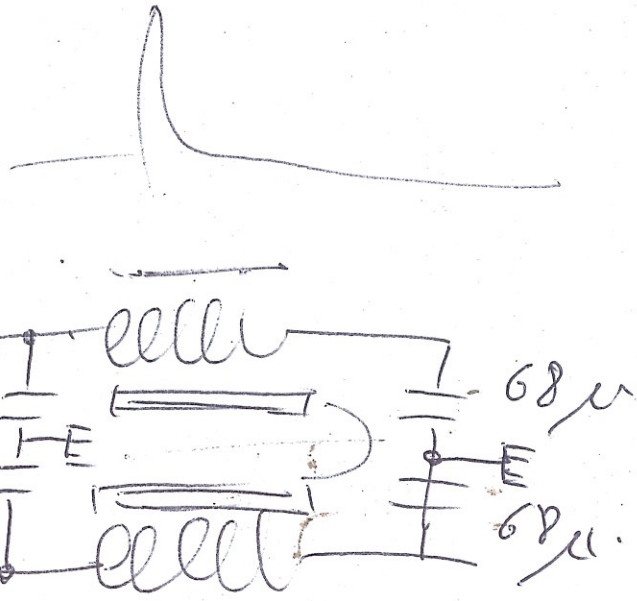
$\Rightarrow$ C bypass.





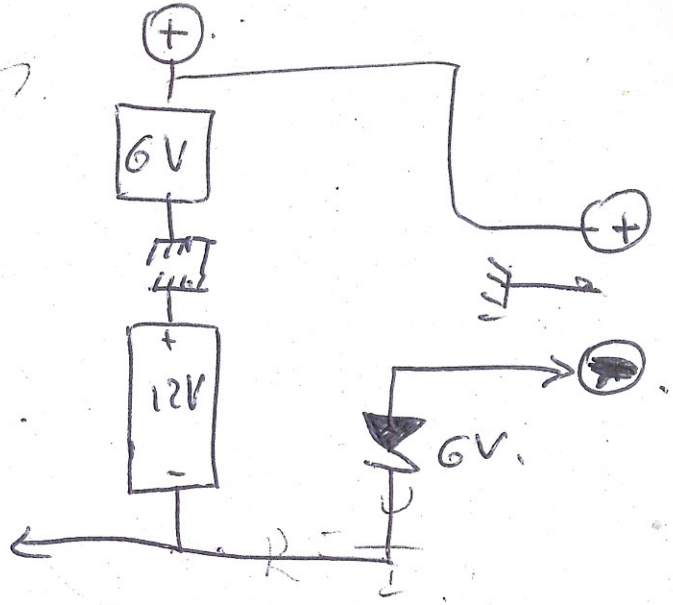






50kΩ.

I = 25mA.



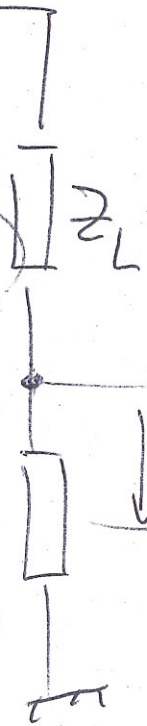
3V.

$Z_L = \frac{3}{0,025.}$

$= 120\ \Omega$

6V.

0,38mH.

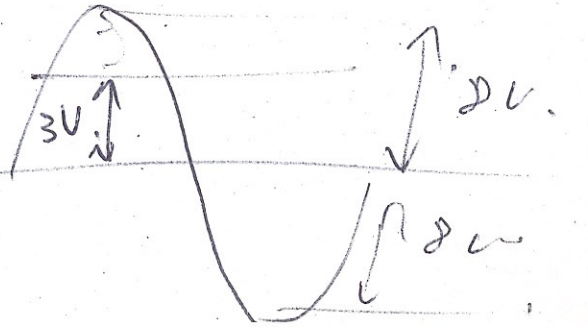


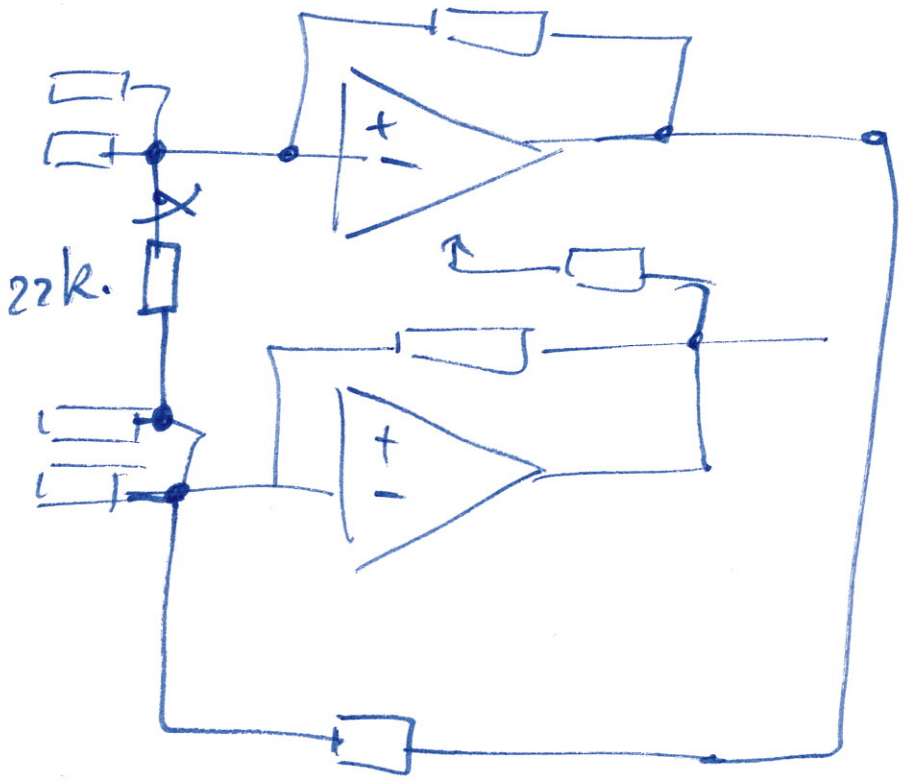
$Z_C = 600\ \Omega.$

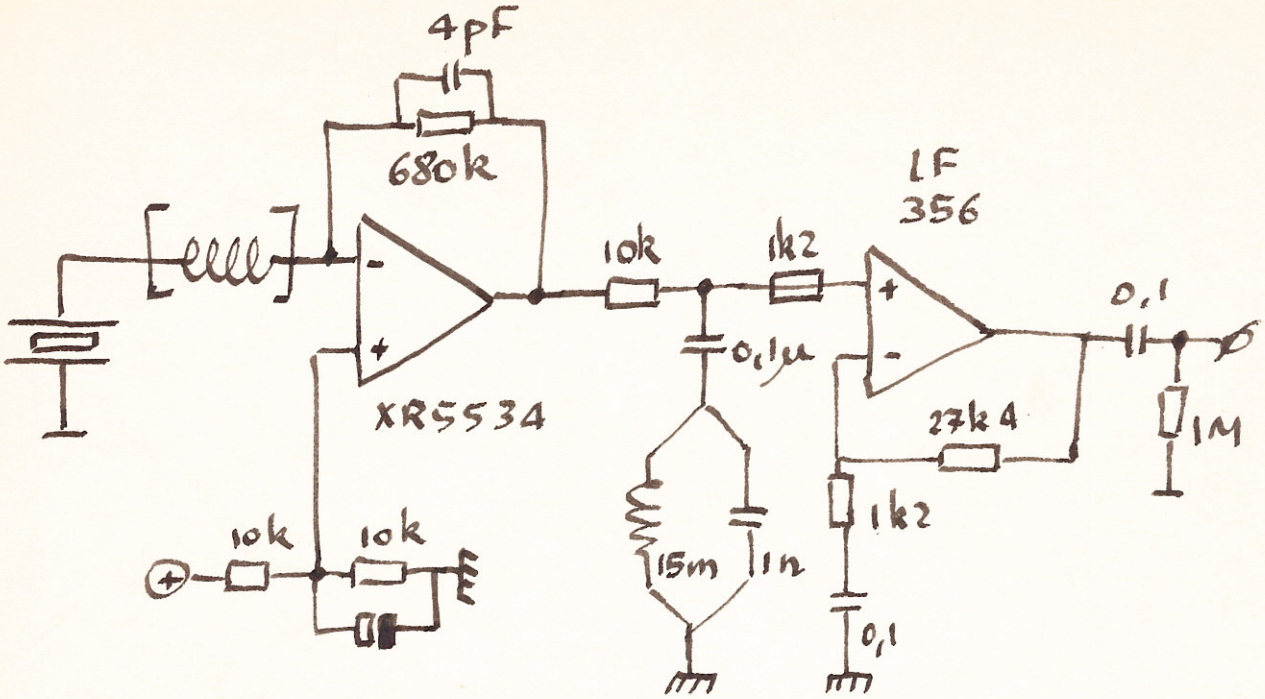
$Z_C = 2\pi f L$

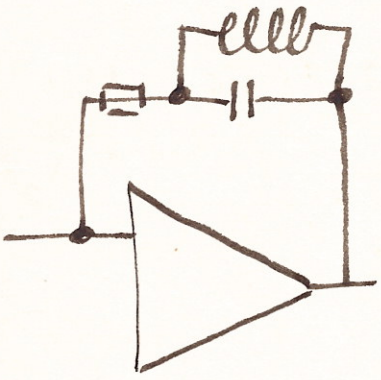
$120 = 2\pi\ 50.10^3 . L.$

$L = \frac{120}{2\pi\ 50.10^3}$

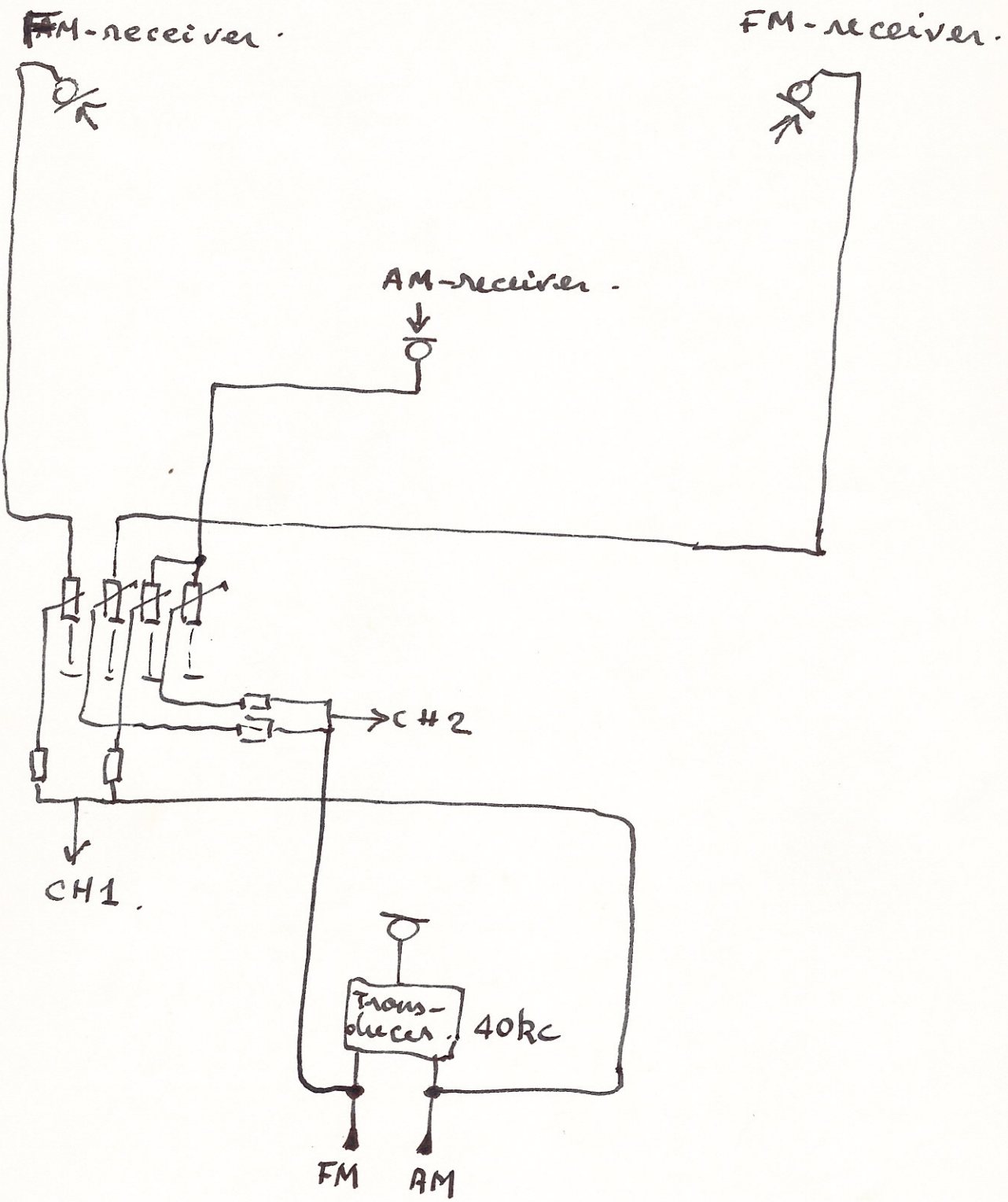



22k.


4pF
680k
LF
356
10k
1k2
0,1
0,1µ
XR5534
27k4
1M
1k2
10k
10k
15m
1n
0,1



Holosound - Stereo versie.



03/85.

STICHTING LOGOS
instelling van openbaar nut
Kongostraat 35
B-9000 Gent
tel. 091-23.80.89

STUDIO STANDAARDEN :

1. Voedingsaansluitingen met DIN-plug.

buitenaanzicht
DIN-chassisdeel

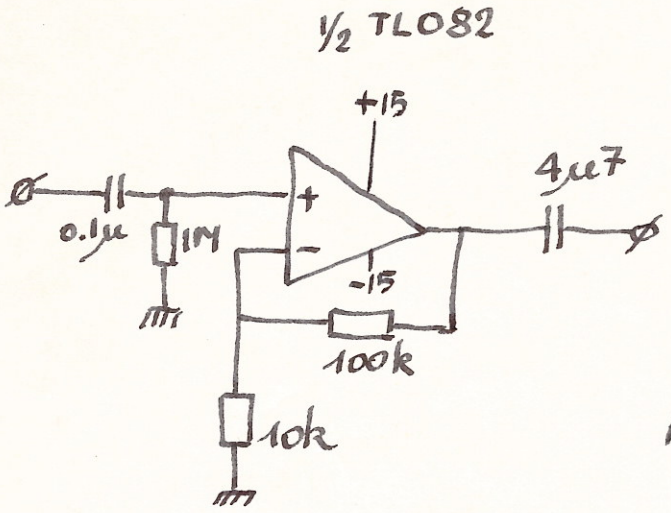
1 = +
2 = 0
3 = −

symmetrische voedingen!

aanzicht soldeerzijde

Quad 20dB-amps

~4 channel~



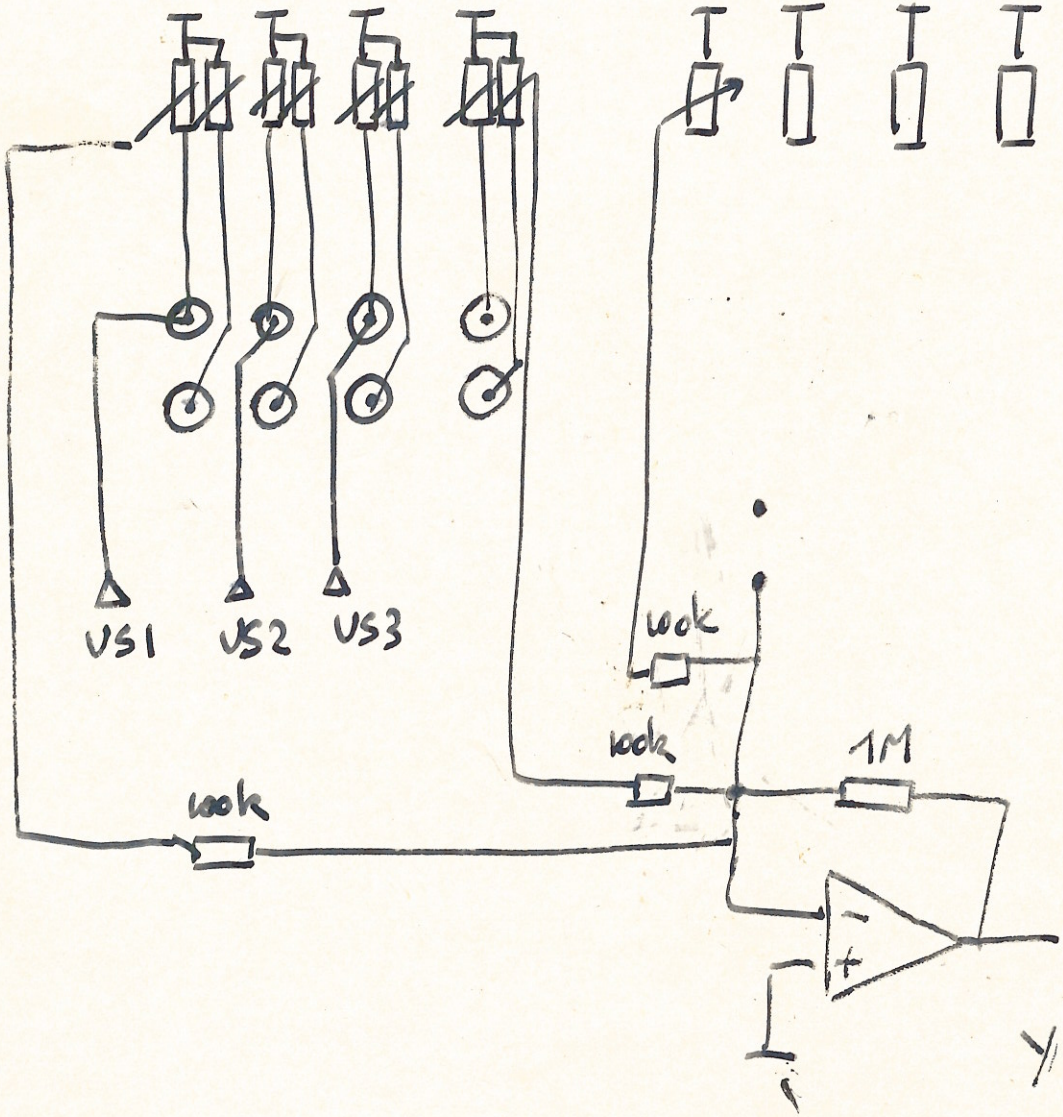
$A_V = 1 + \frac{100}{10} = 11x$

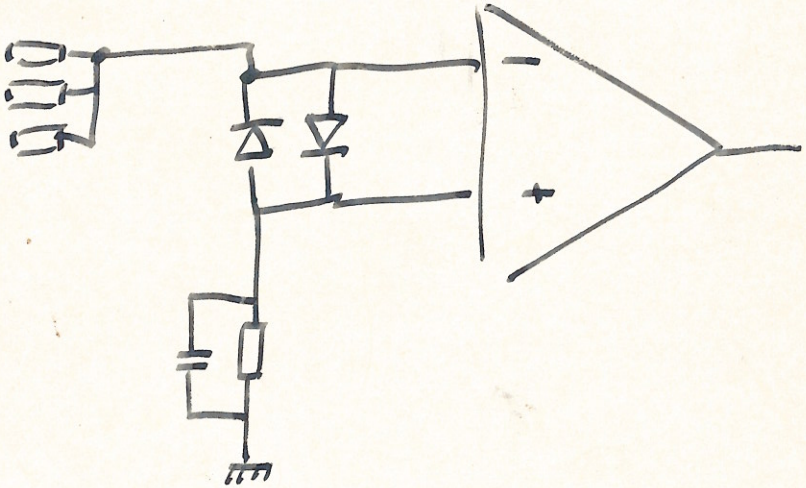
4x mono jack-in ⇒ 2 x Stereo jack Out

$Z_i = 1\,M\Omega$

$V_{i\,max} = 0dB \quad (771mV)$

$(V_o = 8{,}48V)$





0dB ⇒ 10x mit.!

	Stereo	Quad
offset voltages: 1 :	45 mV	177 mV
2 :	21 mV	167 mV
3 :	131 mV	132 mV
4 :	144 mV	140 mV
5 :	−272 mV	−272 mV

MIXER

Maximaal onvervormd uitgangssignaal : $20V_{pp}$.
(bij $U_v = \pm 15V$)

$U_o = 7$ Volt$_{rms}$

→ maximaal ingangssignaal recovery-amp, busline mixer: $\frac{U_o}{A_v} = \frac{7}{12} = 0{,}58 V_{rms}$

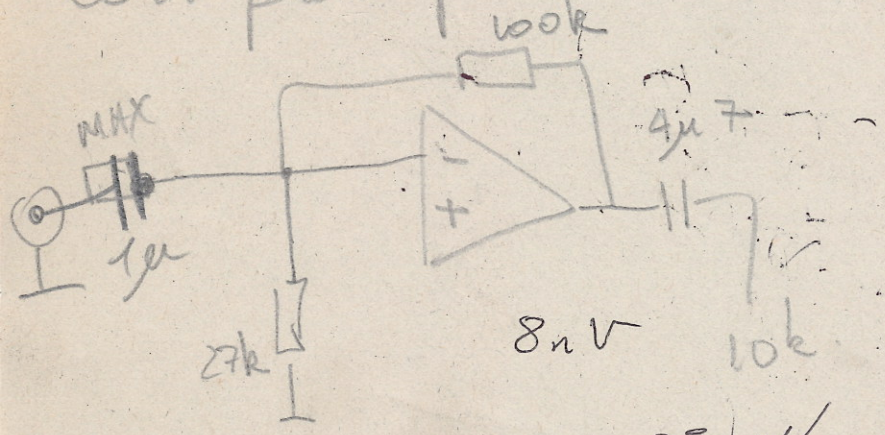
→ Maximaal ingangssignaal op ingangen (bij potmeters in maximale positie): $0{,}58 V_{rms} \times 3{,}15 =$

3,15 = mixerverzwakkingsfaktor

$1{,}827 V_{rms}$

Timiframes driver ???

Coil preamp:



16 Hz

$25 nV/\sqrt{Hz}$.

$f_o = \frac{1}{2\pi RC}$

$\frac{1}{6{,}28 \cdot 10^5 \cdot 0{,}1\, 10^{-6}}$

~~6,28~~ 6,28 · 0,1 6,28

3-dim. oscillator. driver

berekeninpen
met-inpen
ontwerp.

06/84

ca. 1kHz

775mV - 0dB

input (1) out: 246mV

op LS-out: 760mV
(onbelast!)

belast 8 Ω: 267mV

belast 800 Ω: 732mV

0dB op MIC-in (1) (rechts) out: 219mV

out: 2 → 1,86V

---

op open LS-out

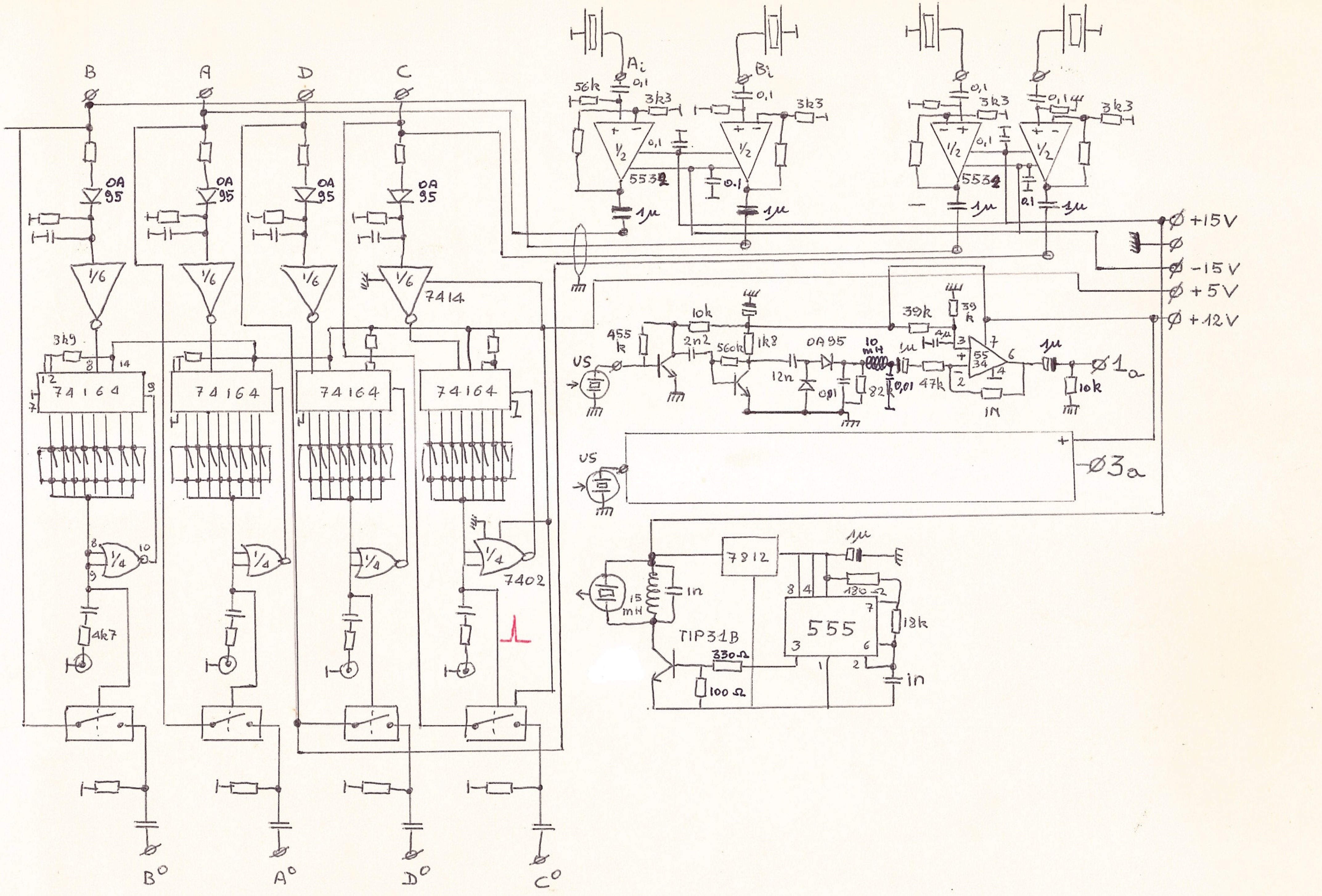
f/2	1,86 V
f/3	1,53
f/4	1,13
f/5	912mV
f/6	774mV
f/7	675mV
f/8	600mV
f/5	913mV
f/3	1,53V
1f	53mV
of	2mV - ruis
STIL	0,000 V

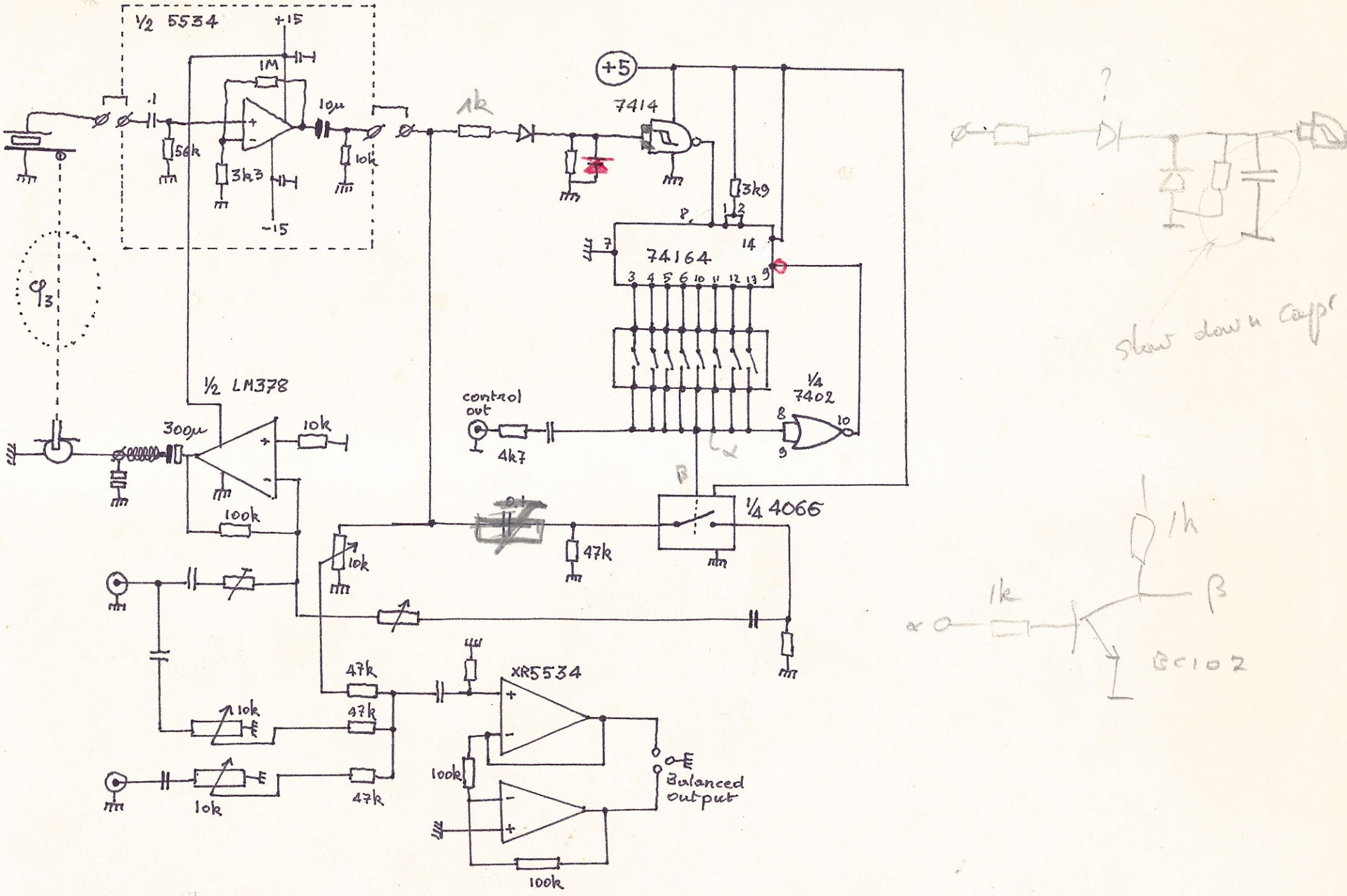
f: 1 uitgang sloor aan als

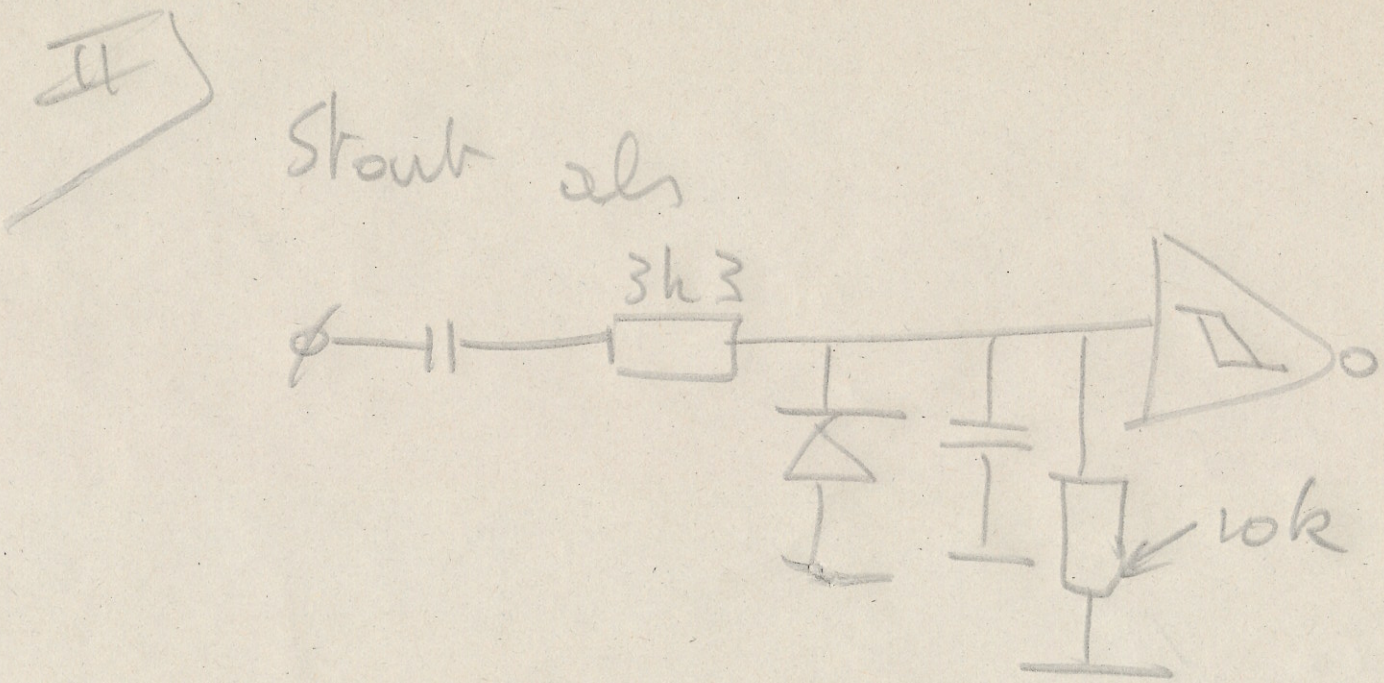
$U_{in\ RMS} \geq 1{,}5V$

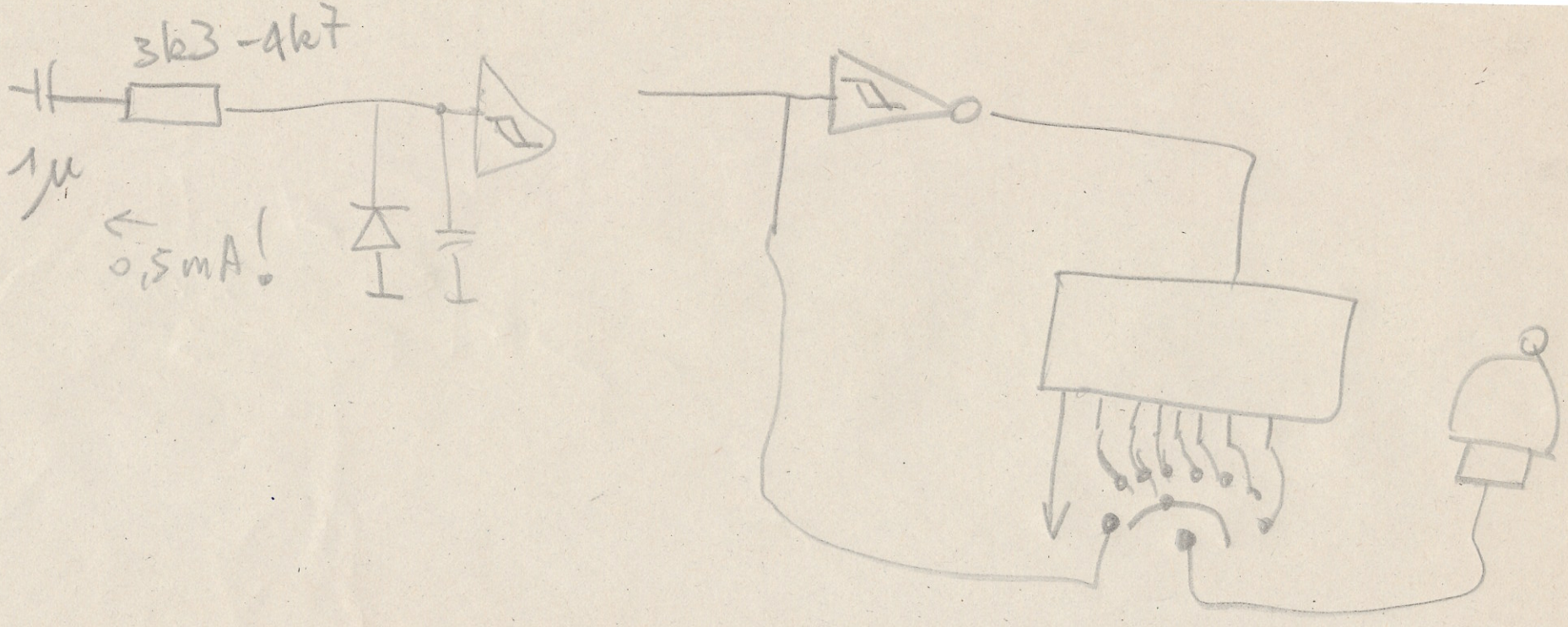
f: n uitgangsloor aan als

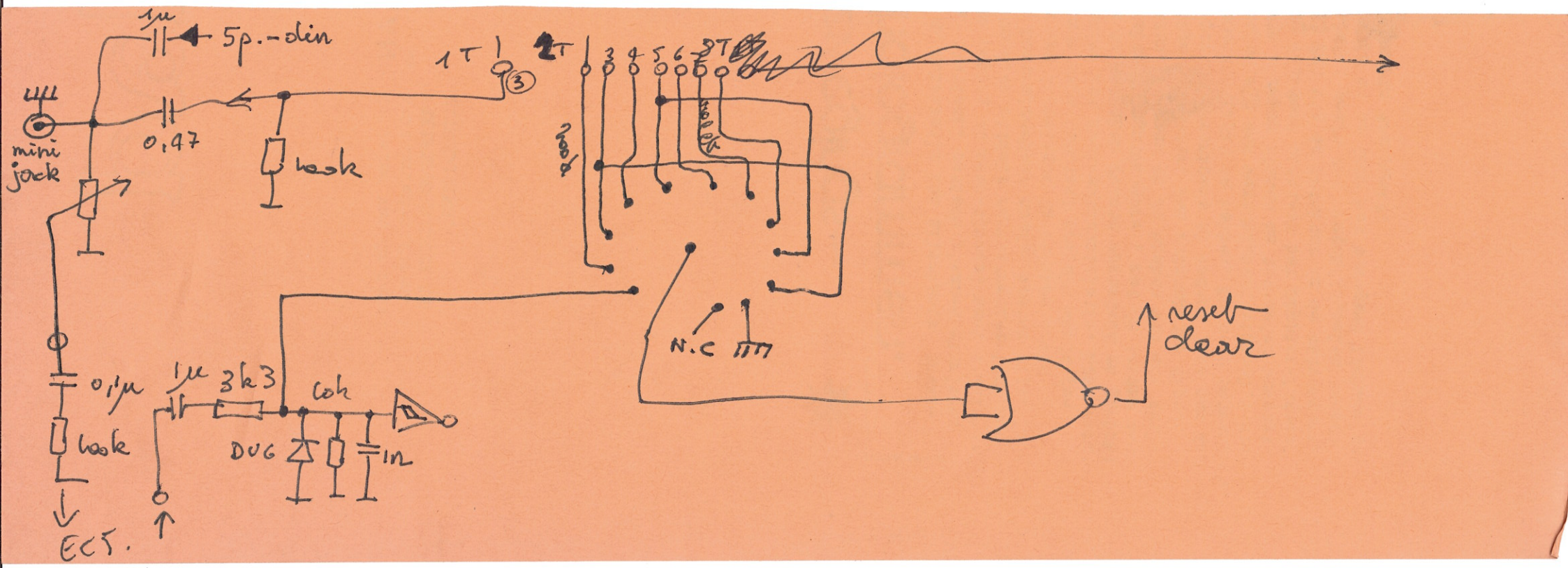
$U_{in\ RMS} \geq 375mV$


B
A
D
C
OA 95
1/6
7414
3k9
74164
1/4
7402
4k7
B°
A°
D°
C°
Ai
Bi
56k
0,1
3k3
1/2
5532
1μ
0,1μ
+15V
-15V
+5V
+12V
US
455 k
10k
2n2
560k
1k8
12n
OA95
0,01
10 mH
82
39k
39 k
4μ
47k
55 34
1M
10k
1a
3a
7812
555
180 Ω
18k
1n
15 mH
TIP31B
330 Ω
100 Ω

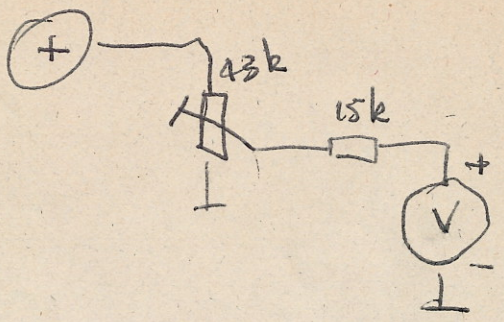

½ 5534
+15
1M
.1
10µ
1k
+5
7414
56k
3k3
10k
-15
3k9
74164
φ3
½ LM378
300µ
10k
control out
4k7
¼ 7402
¼ 4066
100k
47k
10k
XR5534
Balanced output
slew slow n Capr
1k
Bc107


Stout als
3k3
10k

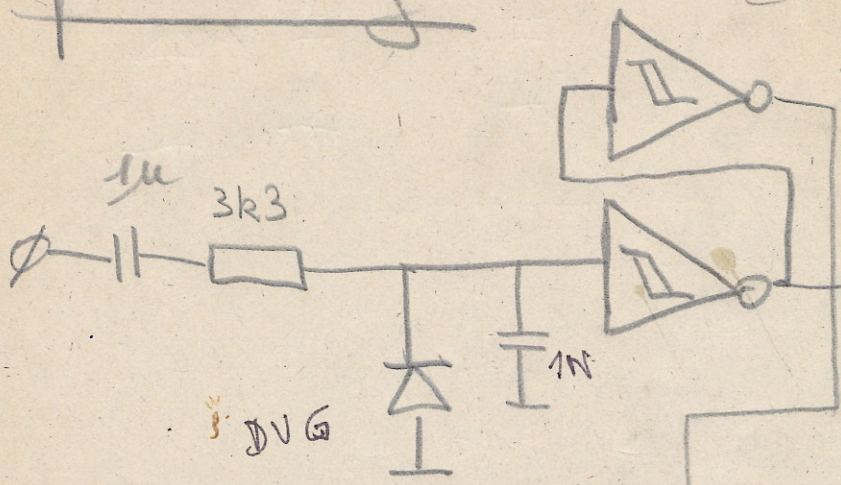

3k3 - 4k7
1µ
0,5mA!

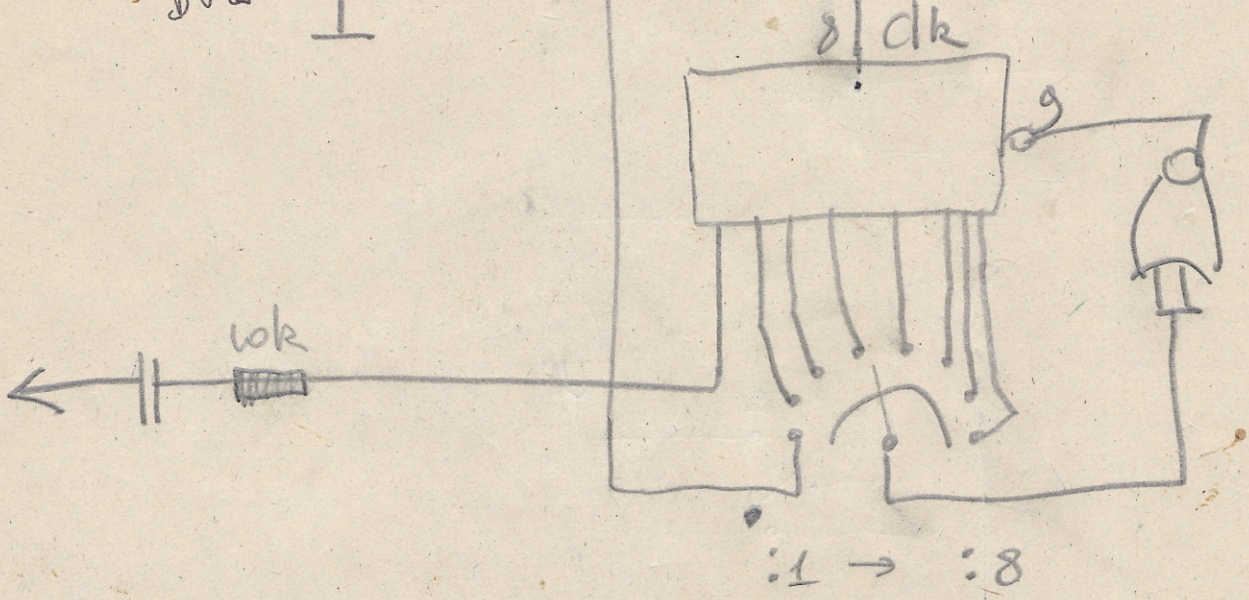

1µ
5p.-olin
1T
2T
3
4
5
6
7T
3
mini jack
0,47
hook
200
N.C
reset clear
0,1µ
1µ
3k3
10k
DUG
1n
hook
ECT.

Oplossing

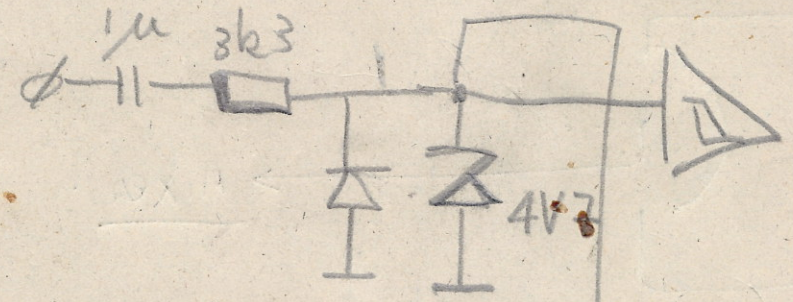


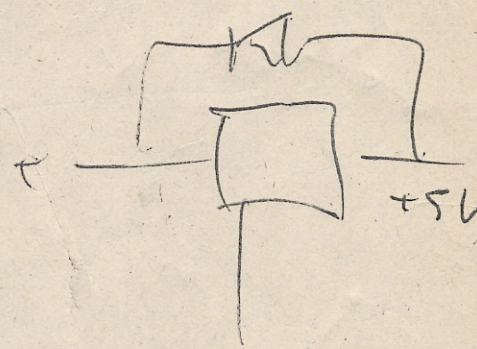
2x



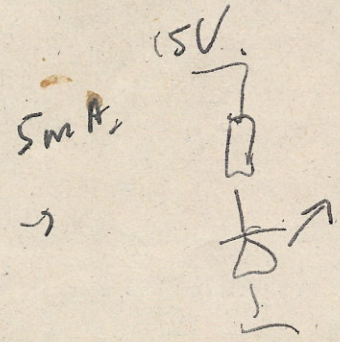


+ 2 x

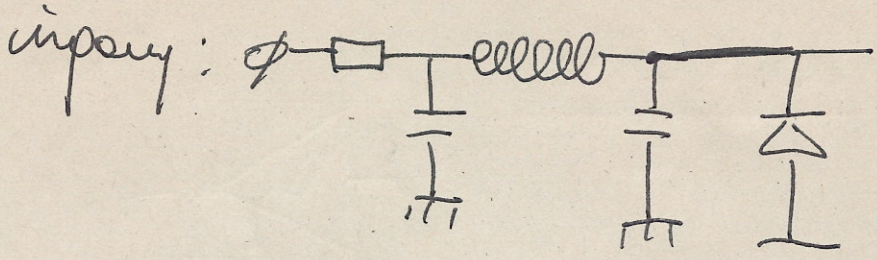


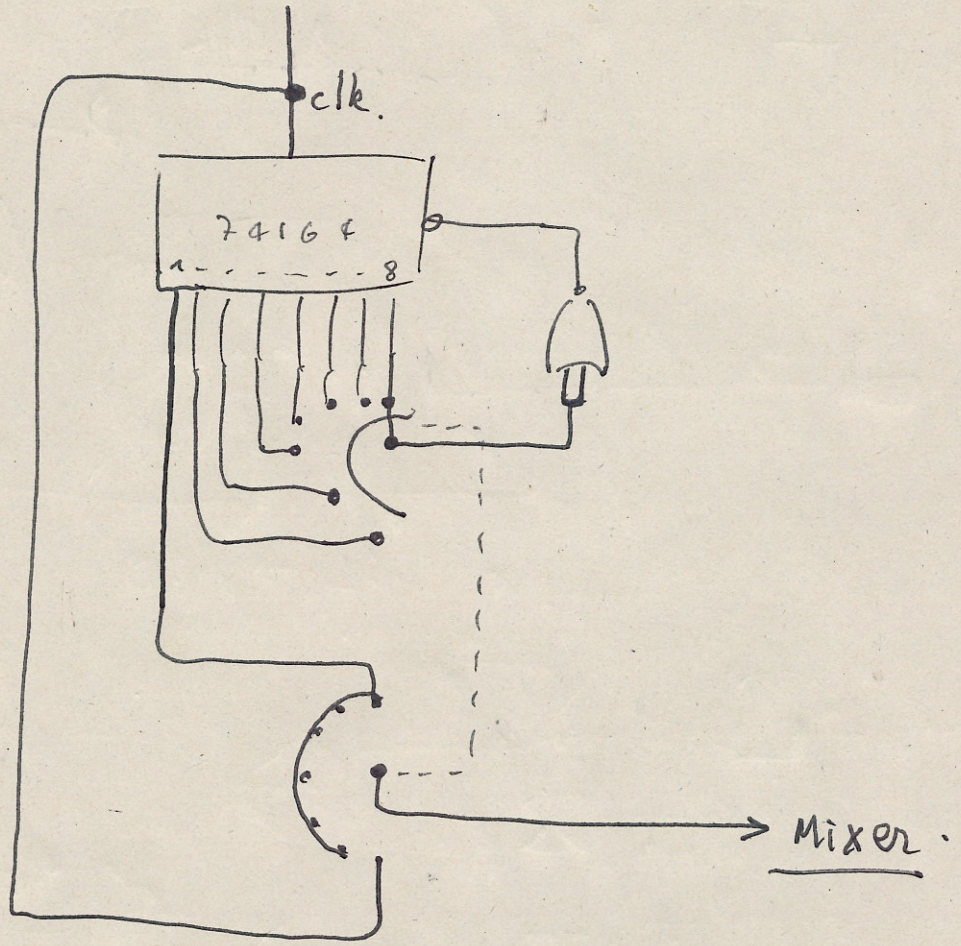


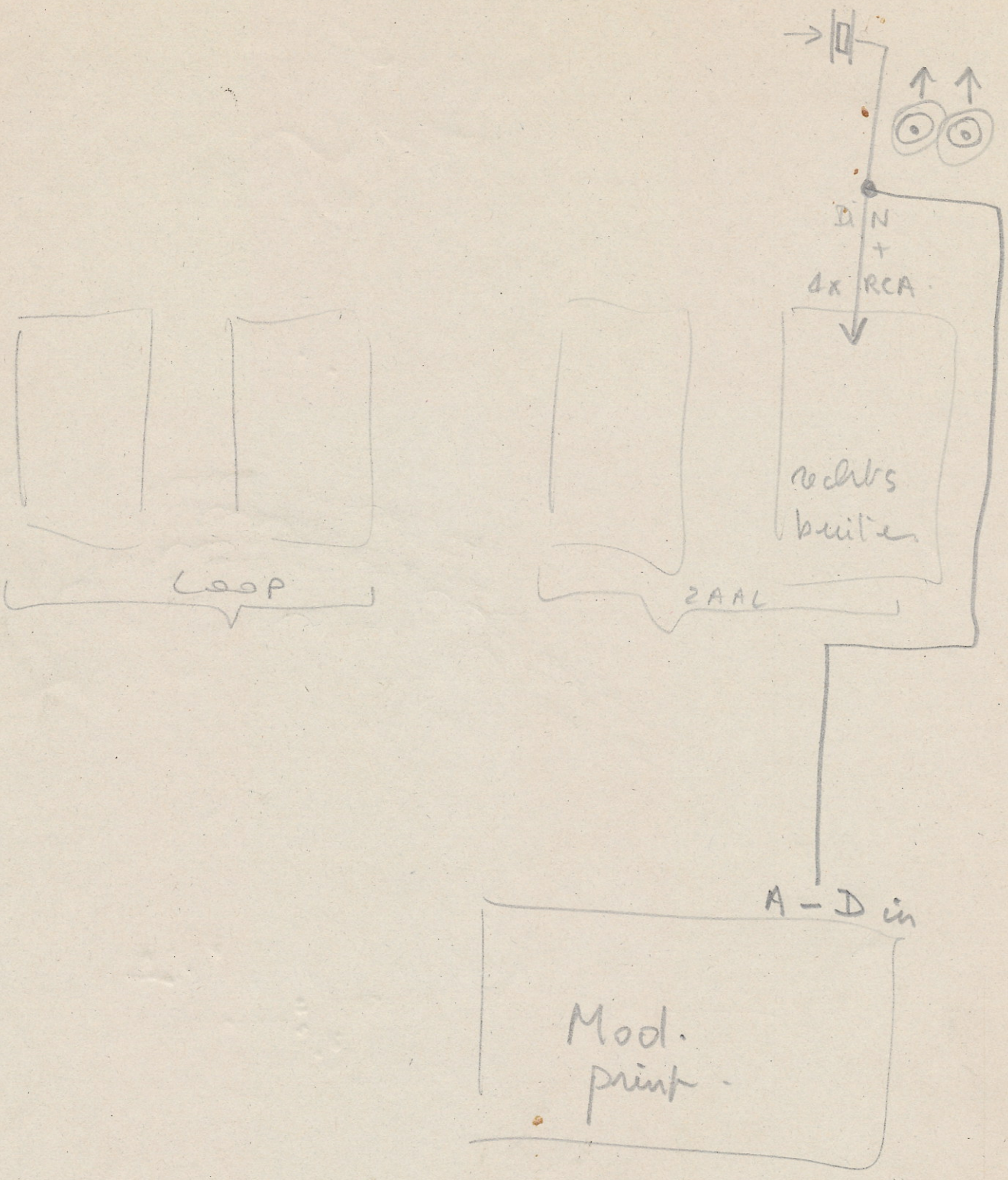
→ sb. 1.



Nuyts
Posman.






DIN
+
4x RCA
Loop
2AAL
A-D in
Mod.
print.

40106 ≠ Nikro-draad

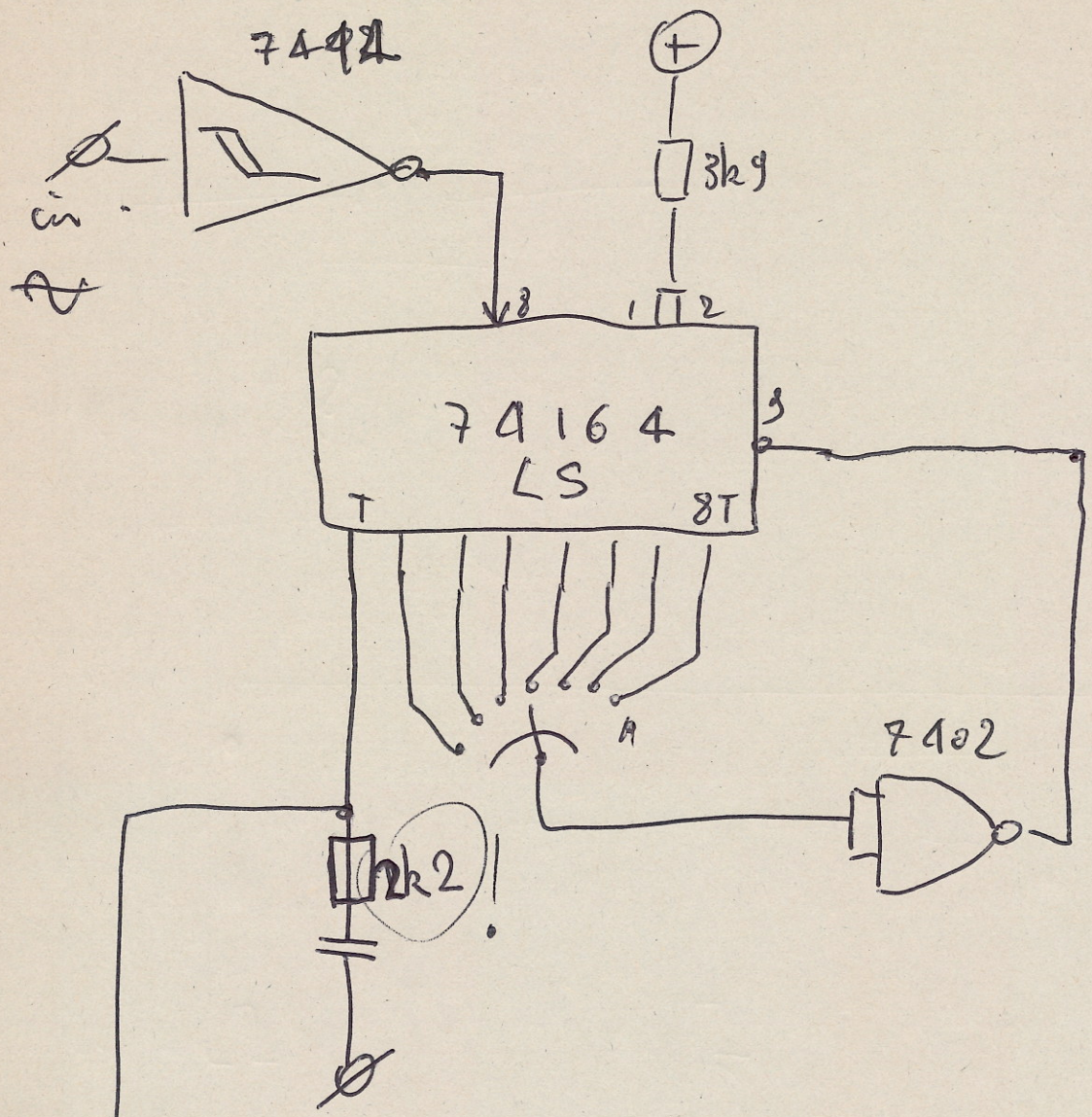
(= 7414)

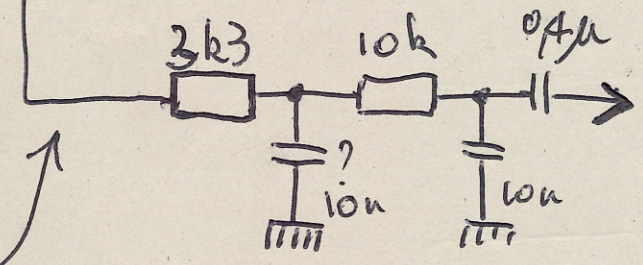
4 draai-schak's

7402 pin 6 pin = 7401

DEUTSCHLANDFUNK - Raderberggürtel 40 - 5000 Köln 51

eindelijk C-mos niet werkend te krijgen is :



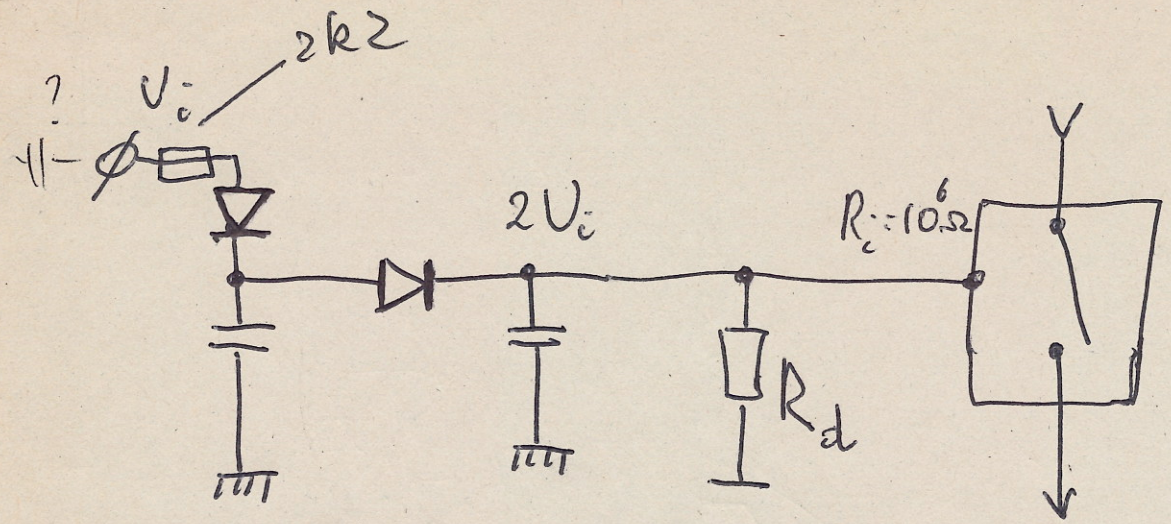


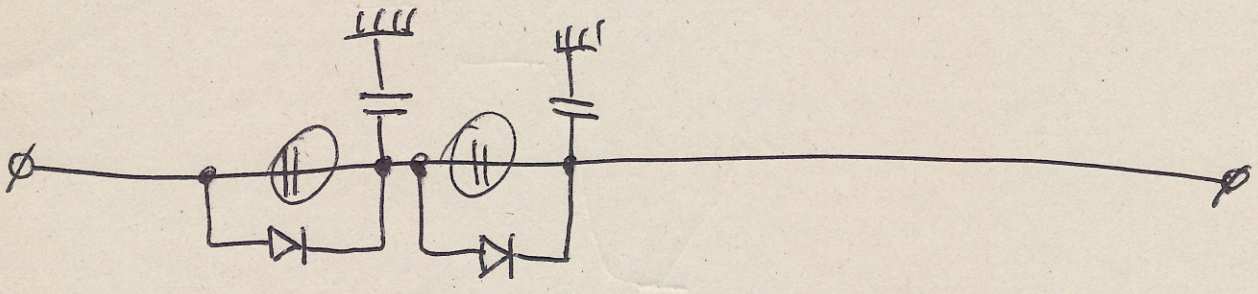
$U_{rms.} \rightarrow \frac{2,6}{2\sqrt{2}} \approx 1\,Volt.$

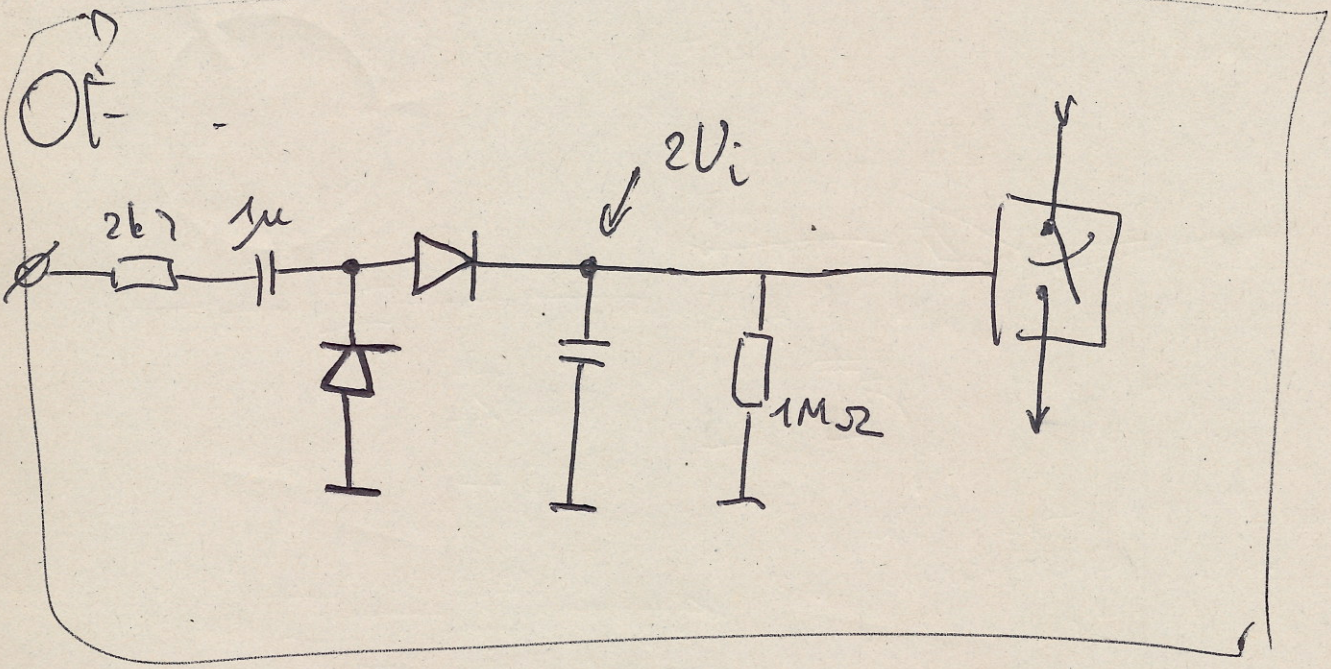
+3 dB level

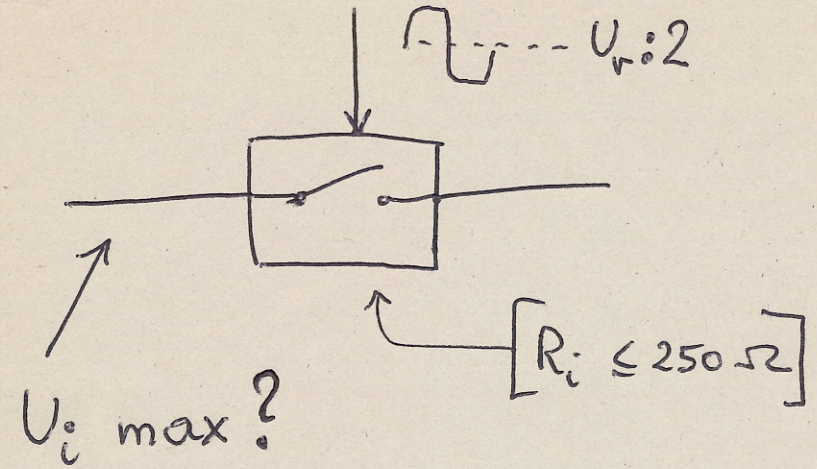
± 2,6 Vpp.

Low-pass !
1kc


?
V_i
2k2
$2V_i$
$R_i = 10^6 \Omega$
R_d
Y



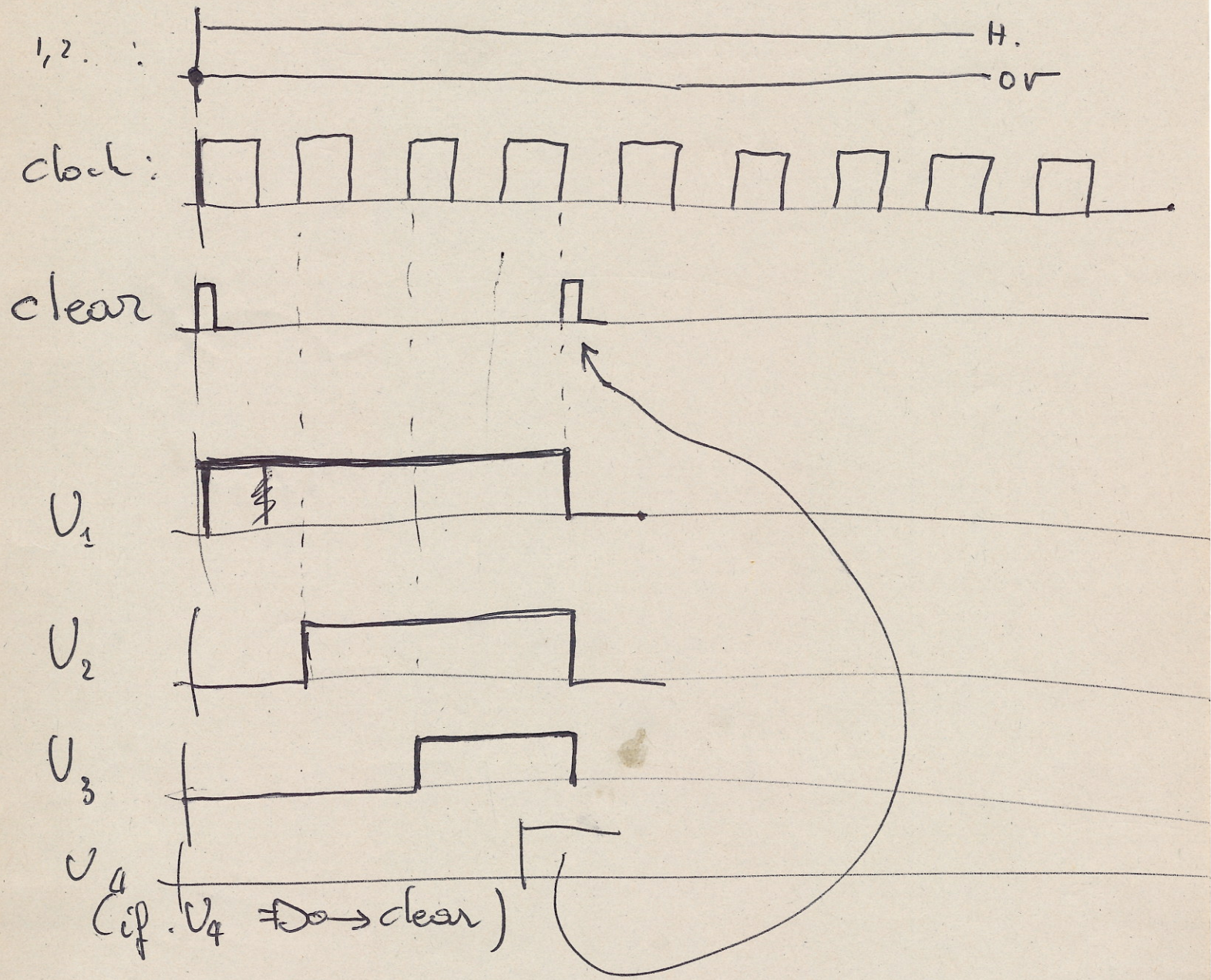

?
2k2
1µ
$2V_i$
1MΩ
Y



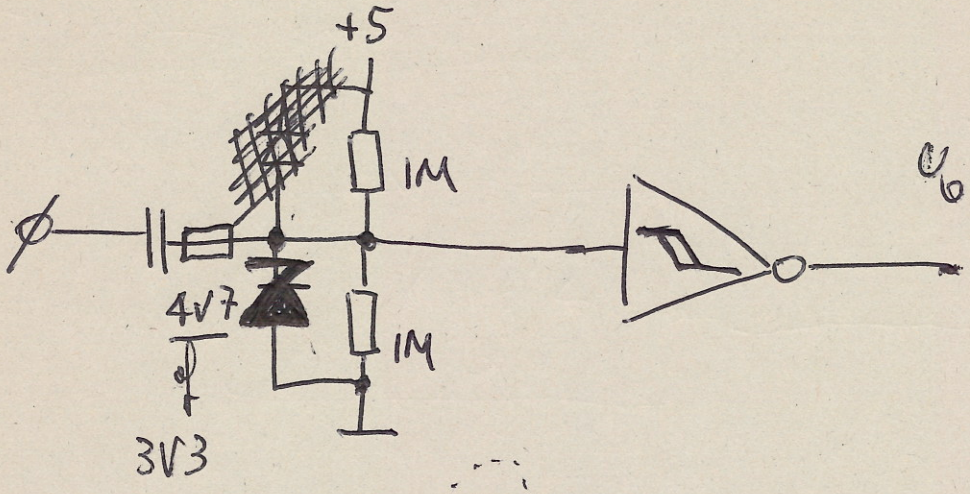
C-mos
4066 schalt.

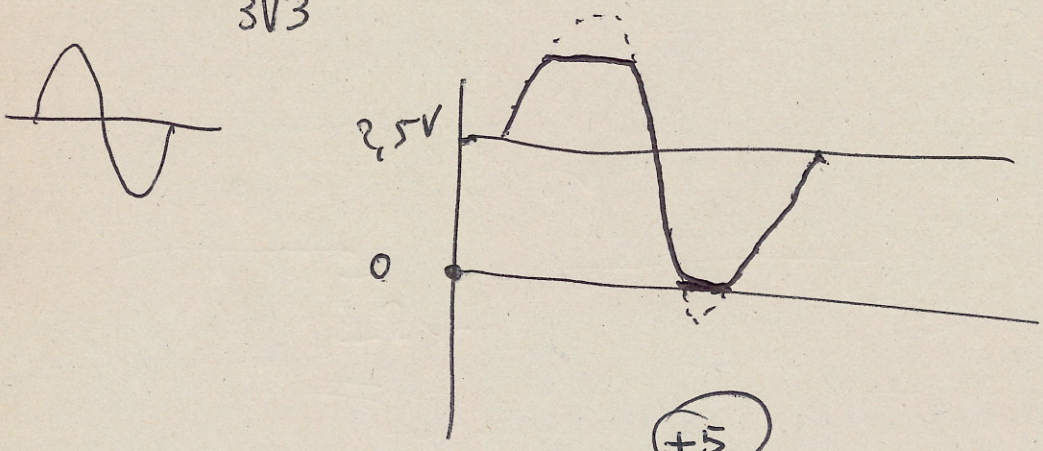
U_i max?

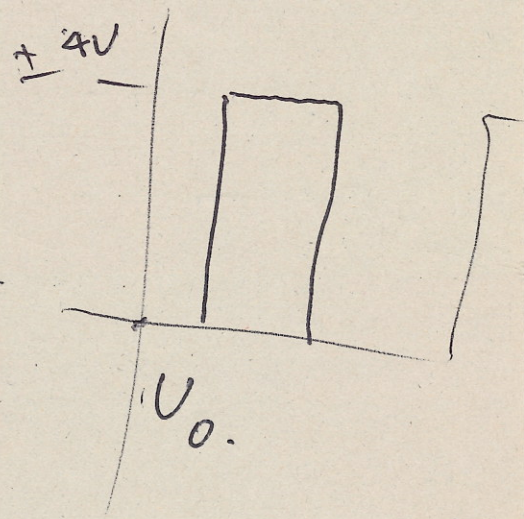
74164.

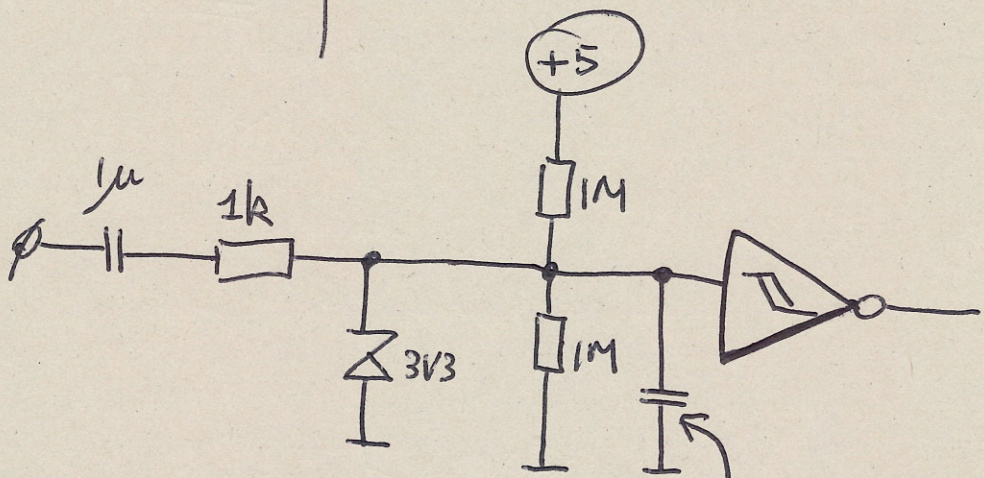


input c-mos Δ !

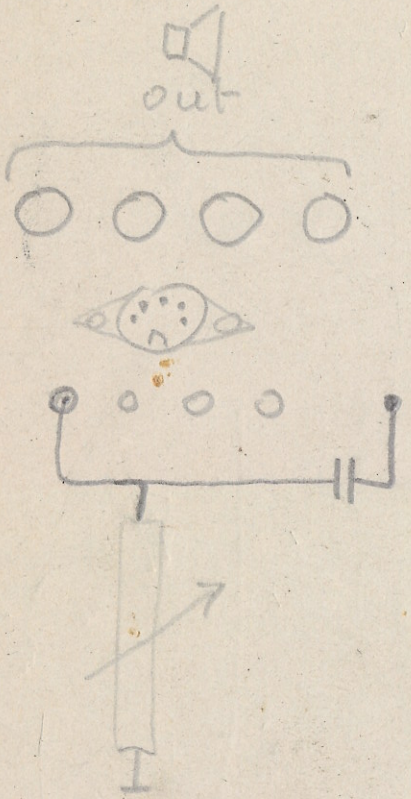


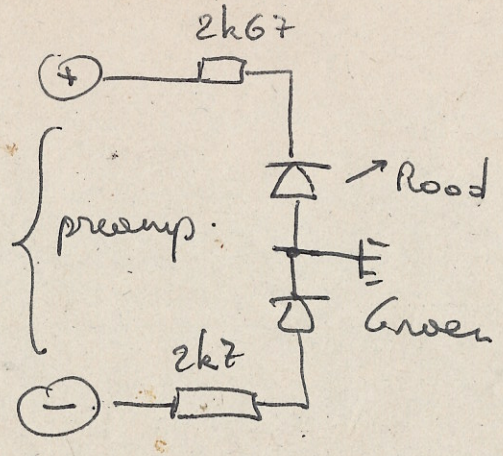


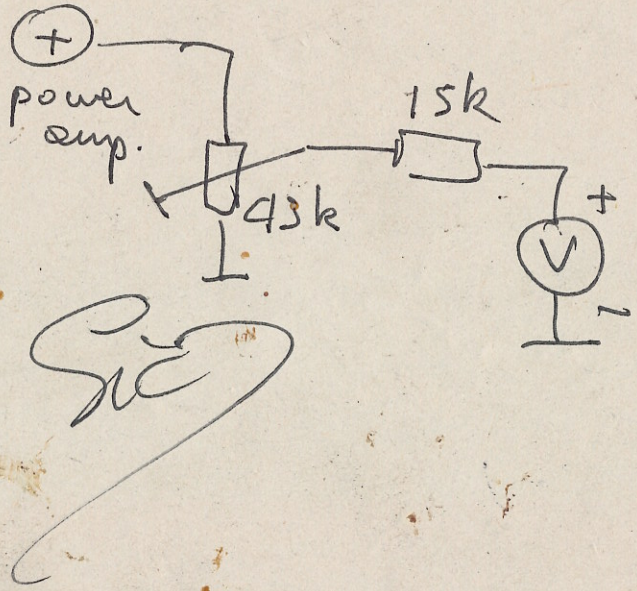




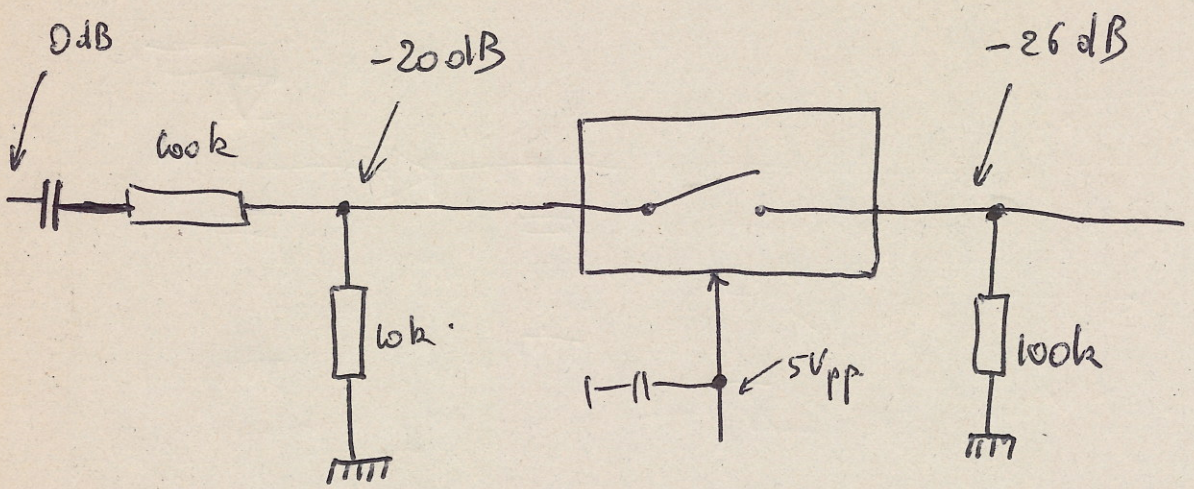
evt. slow-down cap. (integrating)



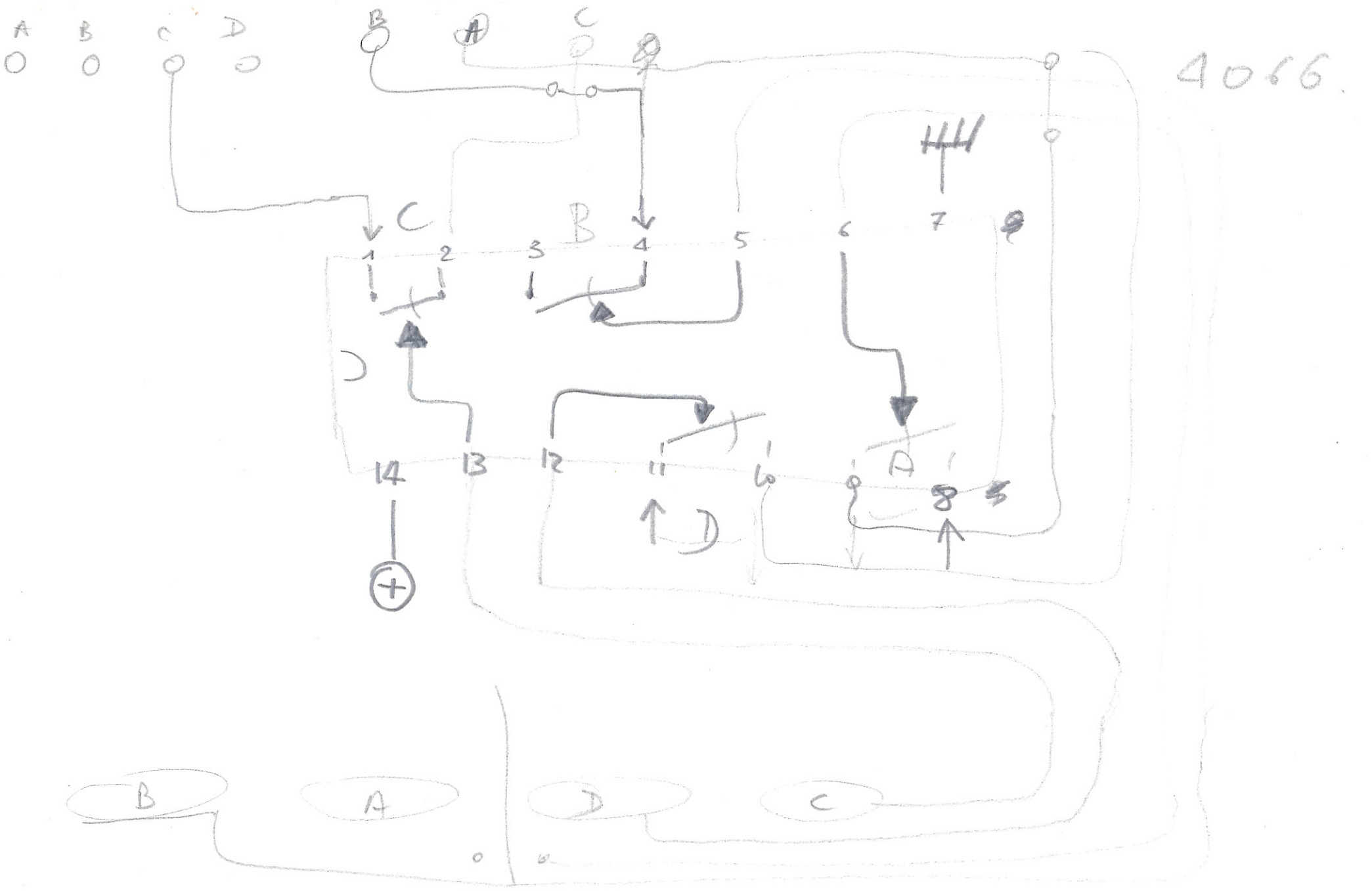


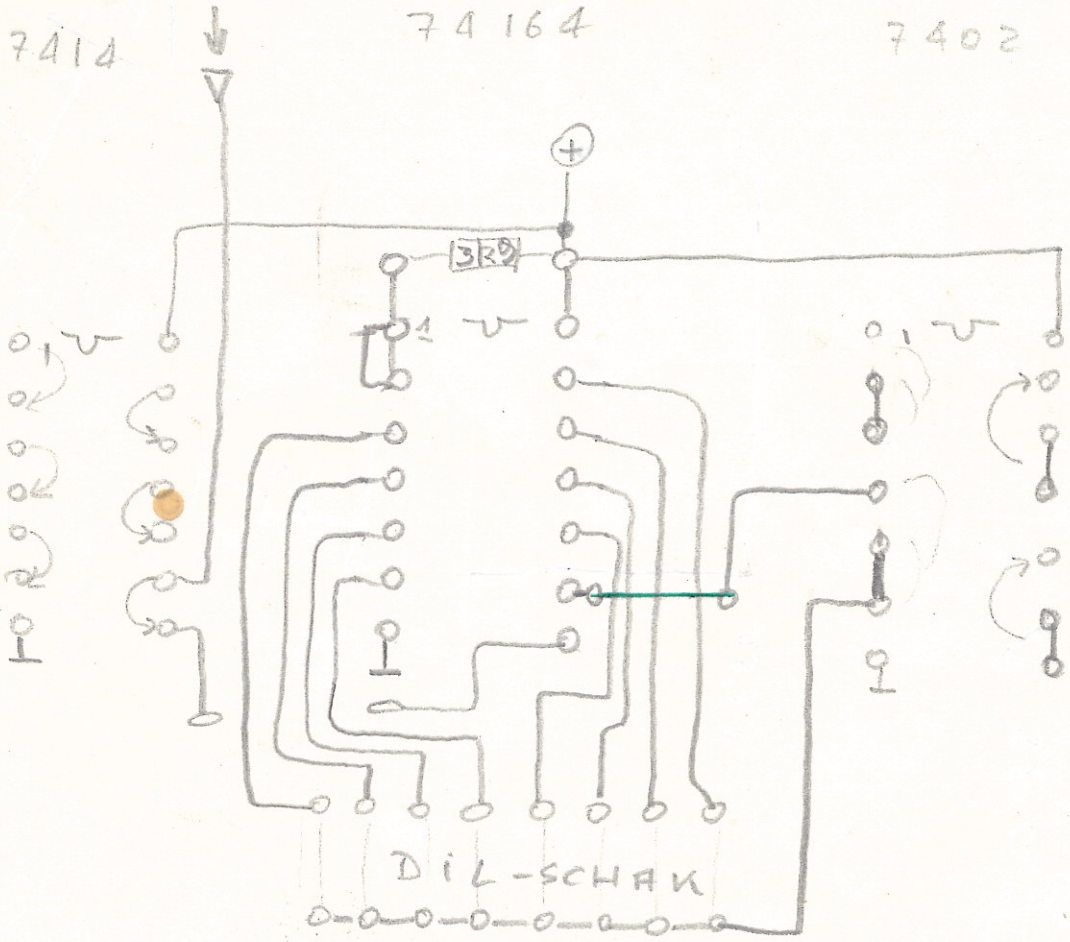


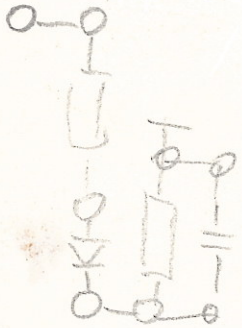
Gradual
- Rackwind
- Fop preops.


0dB
-20dB
-26dB
100k
10k
5Vpp
100k

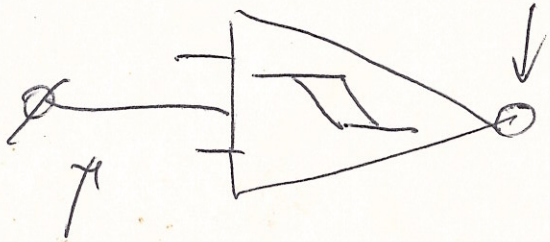
A-1
A-2
A-3
A-4
A-5
I
II
III
IV
V
VI
VII
VIII
IX
X
XI
XII


A
B
C
D
4066
1
2
3
4
5
6
7
8
11
12
13
14
+


7414
74164
7402
3K9
DIL-SCHAK



7414



V_{out} = High = 3,4 V

Low = 0,35 V

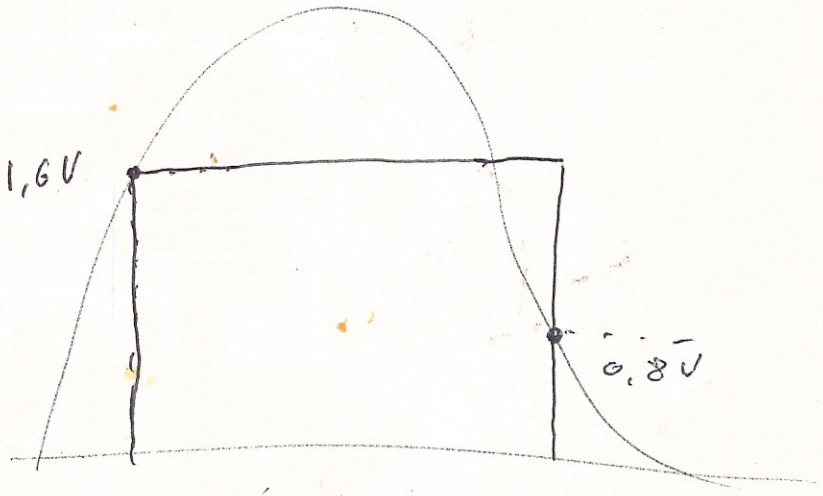
$V_i = 0,14 - 0,18$ mA.

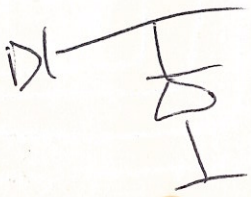
$R = \frac{V}{I}$

0,35 V − 0,18 mA.

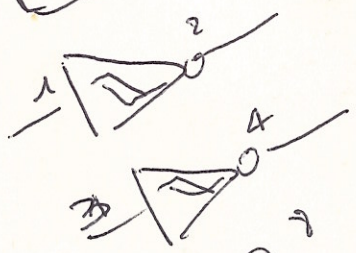
$R_{low} = \frac{0,35}{0,18 \cdot 10^{-3}} = 2k\Omega$

R_{high} =





40106



100kc $100\ s^{-1}$

$100 \cdot 10^{-1}$

$10^{-5}\ s = 2200 \cdot C_1'$

$C_1' = \frac{10^{-5}}{2200}$

$\frac{10^{-5}}{22 \cdot 10^2}$ $\frac{10^{-7}}{22}$

$0{,}045 \cdot 10^{-7}$

$4{,}5 \cdot 10^{-9}\ F$

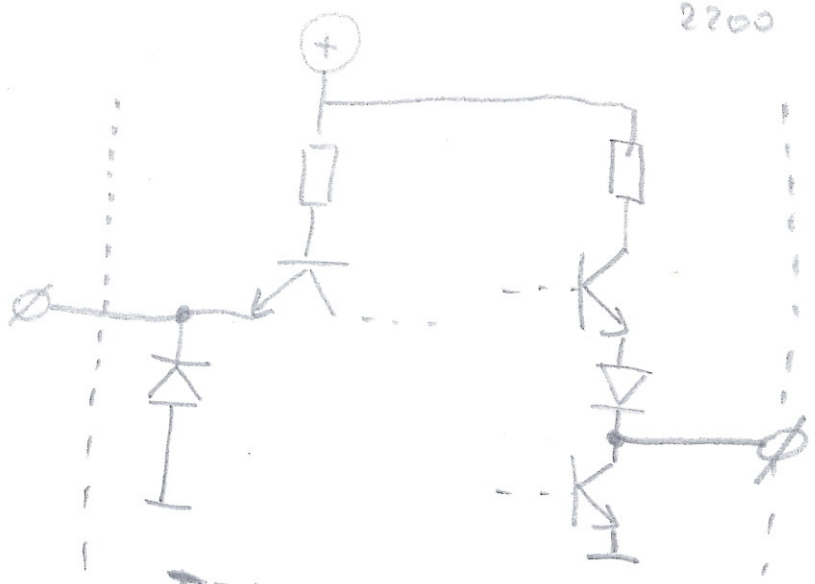
4n5

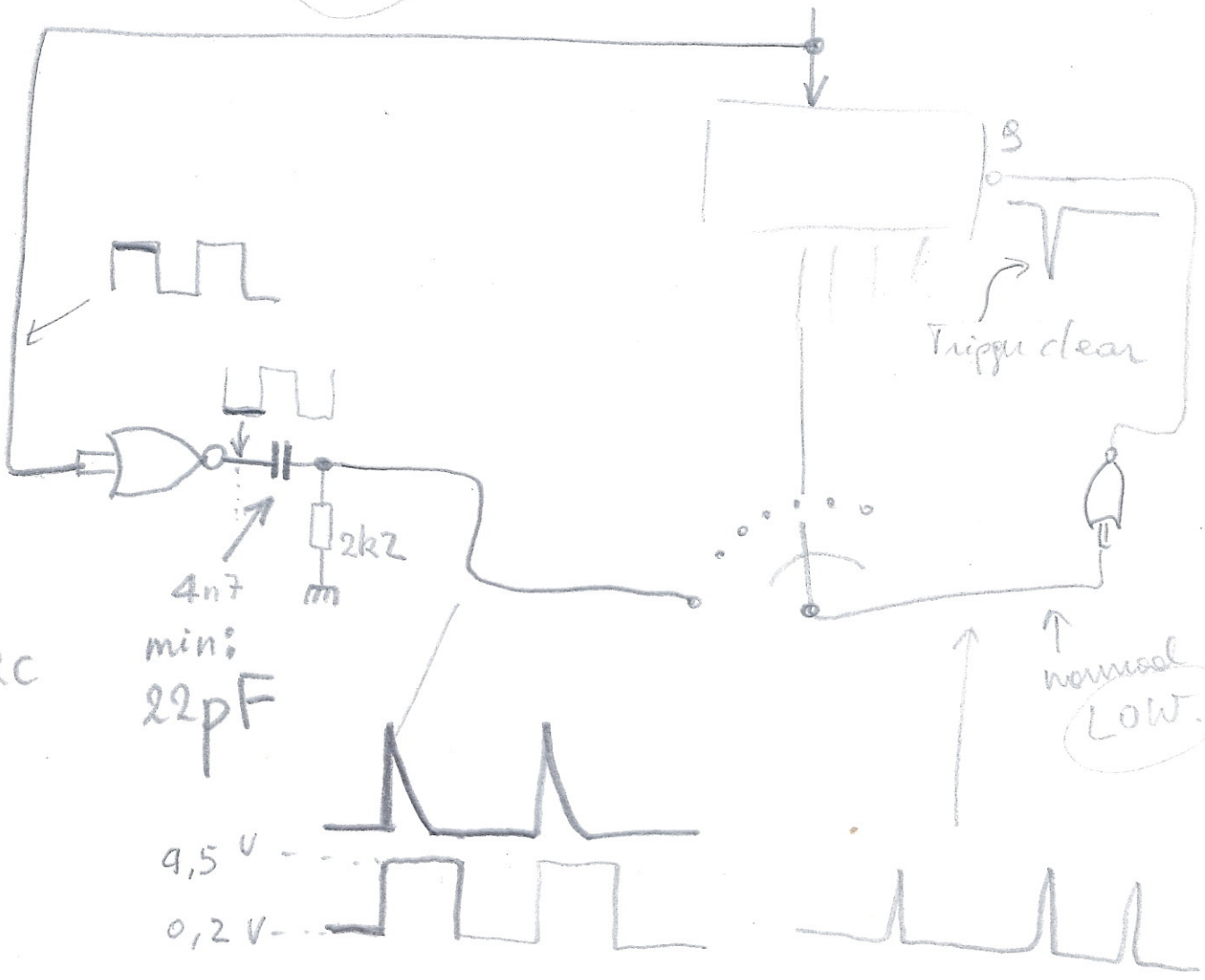
50nS $50 \cdot 10^{-9}\ s$

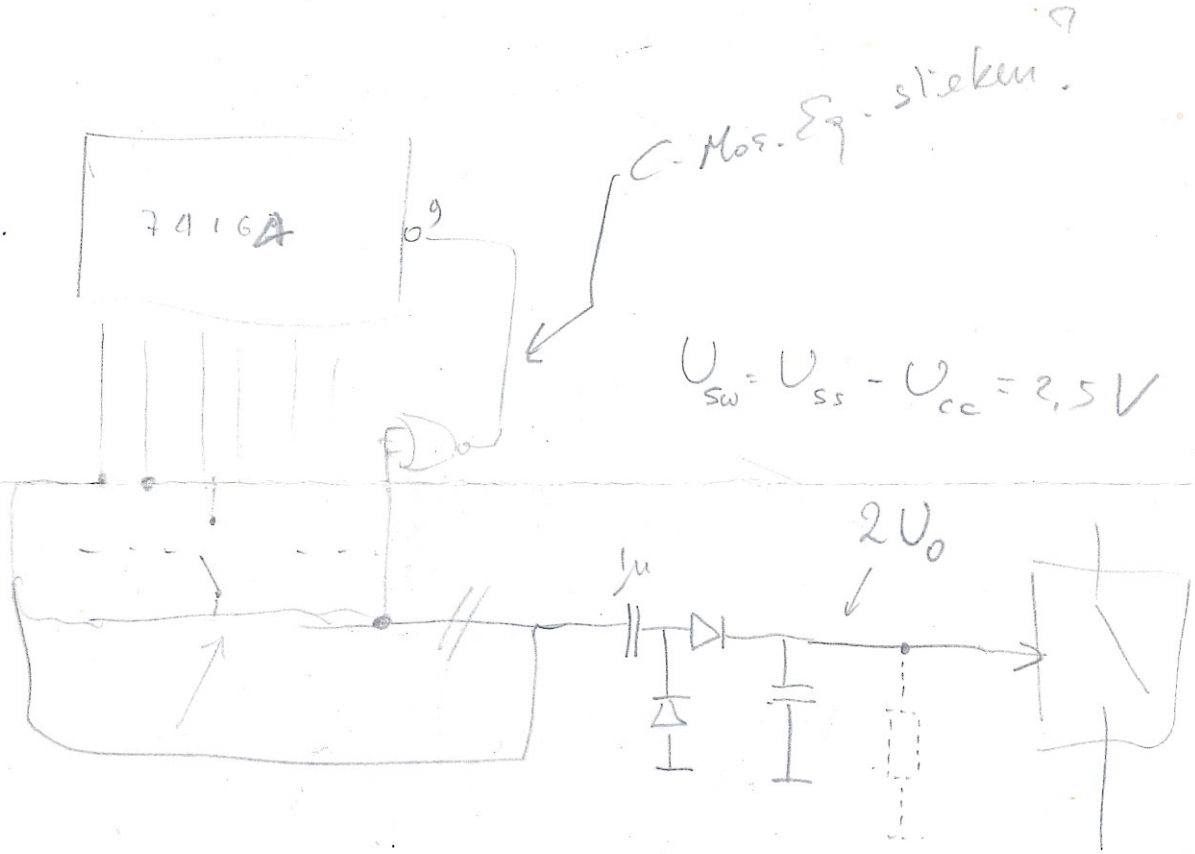
$50\,10^{-9} = 2200\ C_1'$

$C_1' = \frac{50 \cdot 10^{-9}}{2200} = 0{,}022\ nF$

22pF







→ oorzaken fouten

① U_p te klein voor C-mos schak ← bvdc

② & U_p-pulsen te kort ←

③ oversturing ingang ← uitgang schakelaars

④ input Schmitt:
C-mos ⊓ sleken!
puls-to-puls Equiv=

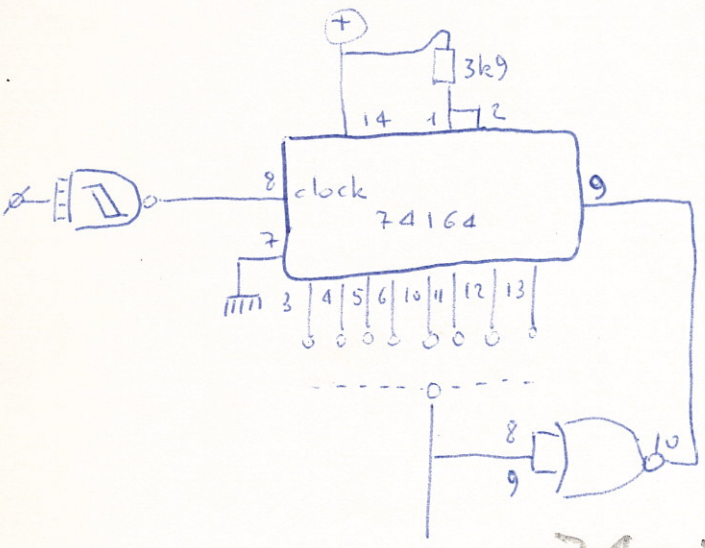
p 216

Monostables.

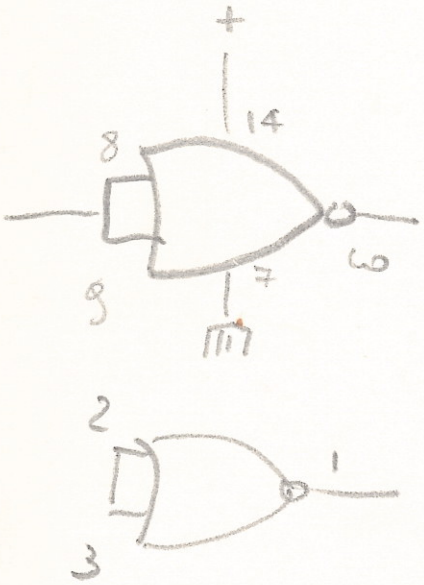
4049 CMOS
4050

74121 TTL
122
123

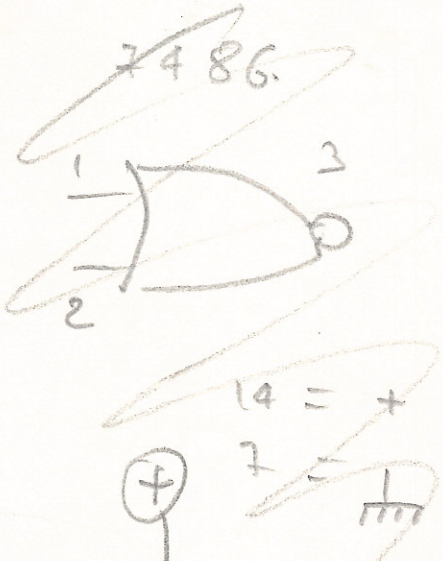
74221 dubbele 74121

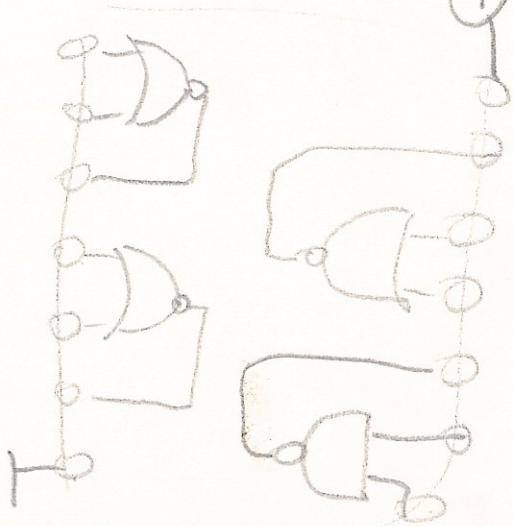


7402



7402





$U_{i\text{-}Mic}$	$U_{i\text{-}progr.}$	mix-bus	U_{out}	$U_{o\text{-}drivers}$ open	$U_{o\text{-}drivers}$ R_L belast	Tripper-level Modulo-n-div.
3,6 V		1,14V		MAX 3,52V		
1,827V	—	0,58V	MAX $7V_{rms}$	1,78V		
—	1,827	"	"			
775mV		246mV		760mV	267mV	OK
375mV		119mV	1,43V			GRENS
						NO —
						NO —
						4

$0dB_{ref.}$

3u30

VOLG-DRECOVERY AMP

TCD : -6 dB mod ~ 160 mV out.

0 dB 320 mV

+6 dB 640 mV

→ 0,5 V - max.

320 mV in → 100 mV op busline

nodig + 1,5 V

→ $A_V = 15x$

voor TCD → 10x.

naar +6 dB-out

$$f_c = \frac{1}{2\pi f}$$

$$Z_c = \frac{1}{2\pi f C}$$

$$\omega = \frac{1}{C}$$

$$f_c = \frac{1}{2\pi C}$$

$$2\pi f = \frac{1}{C}$$

600 Ω

$$600\,\Omega = \frac{1}{2\pi 20 \cdot C}$$

$$600\,\Omega = \frac{1}{125\,C}$$

$$75000\,C = 1$$

$$C = \frac{1}{75000} \quad \frac{1}{75} \cdot 10^3$$

13 µF

Mixer - rechts

Volgversterker - recovery.

0dB in – potmeter op max → bus-line 246mV
775

verzwakking 3x.

→ minimale $A_V = 3x$

voor

0dB in → 0dB out

$U_{out\,max} = 7V_{rms}$.

ca. +18dB

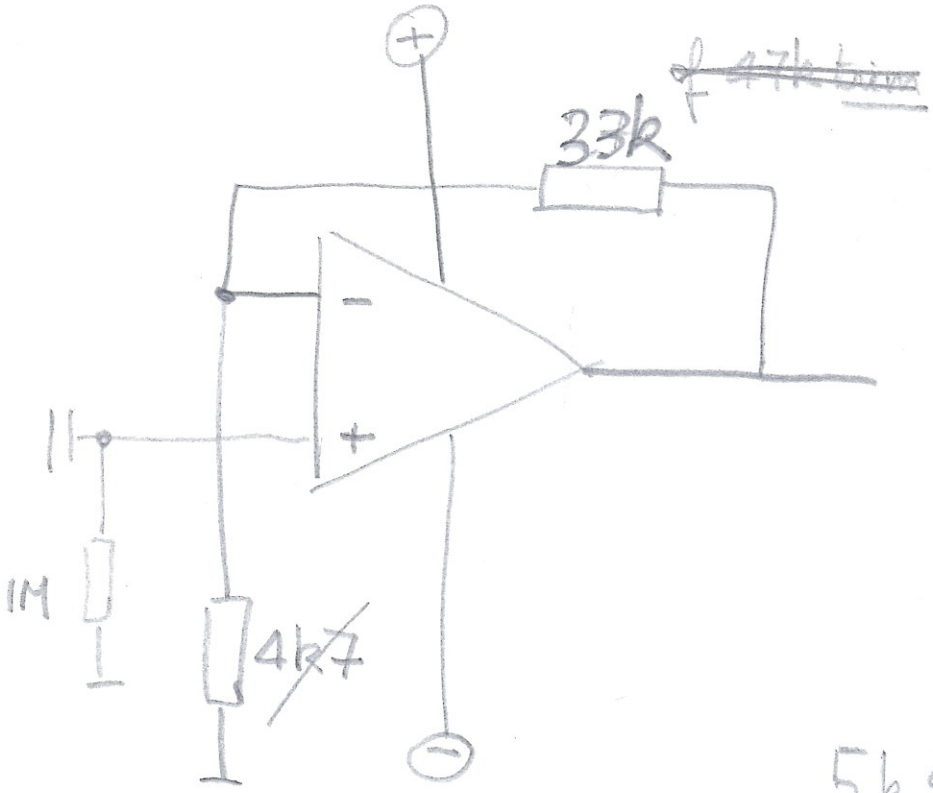
1,55 +6dB
3,1 +12
6,2 +18

als $A_V = 10x$

0dB in
775mV. → 246mV → 2,46V

in: 7,75V 2,46V. x3

Kies $A_V = 6x$.



47k 8,6x

5k49 33k 6x

5k49 5k49 5k49 1x

5k49
Metaal

Output Power?

0dB in →

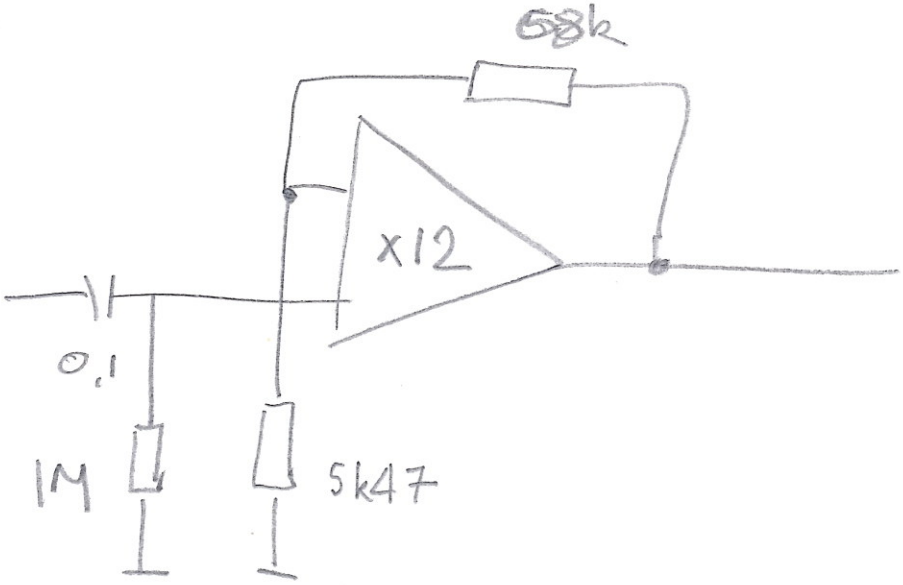
775 mV → 267mV.

|

P = 0,775 V. I

$I = \frac{0,775}{R} = 96mA$

74mW



54k 4 x Metaal

2 op klein 4x

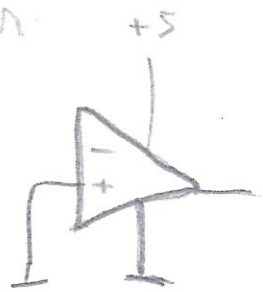
1M 4x

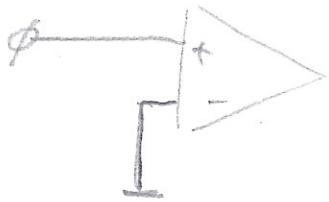
5532

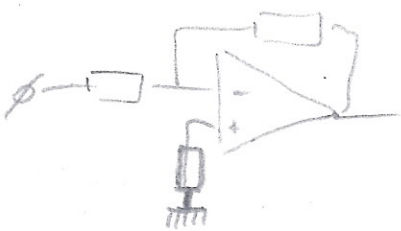
TOV !

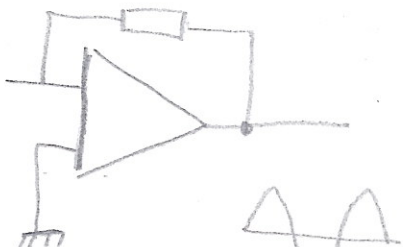
LM 393 = pin t.p.v. 4558.

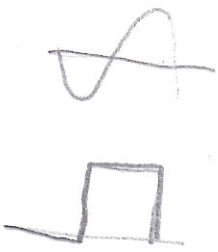
Komparator

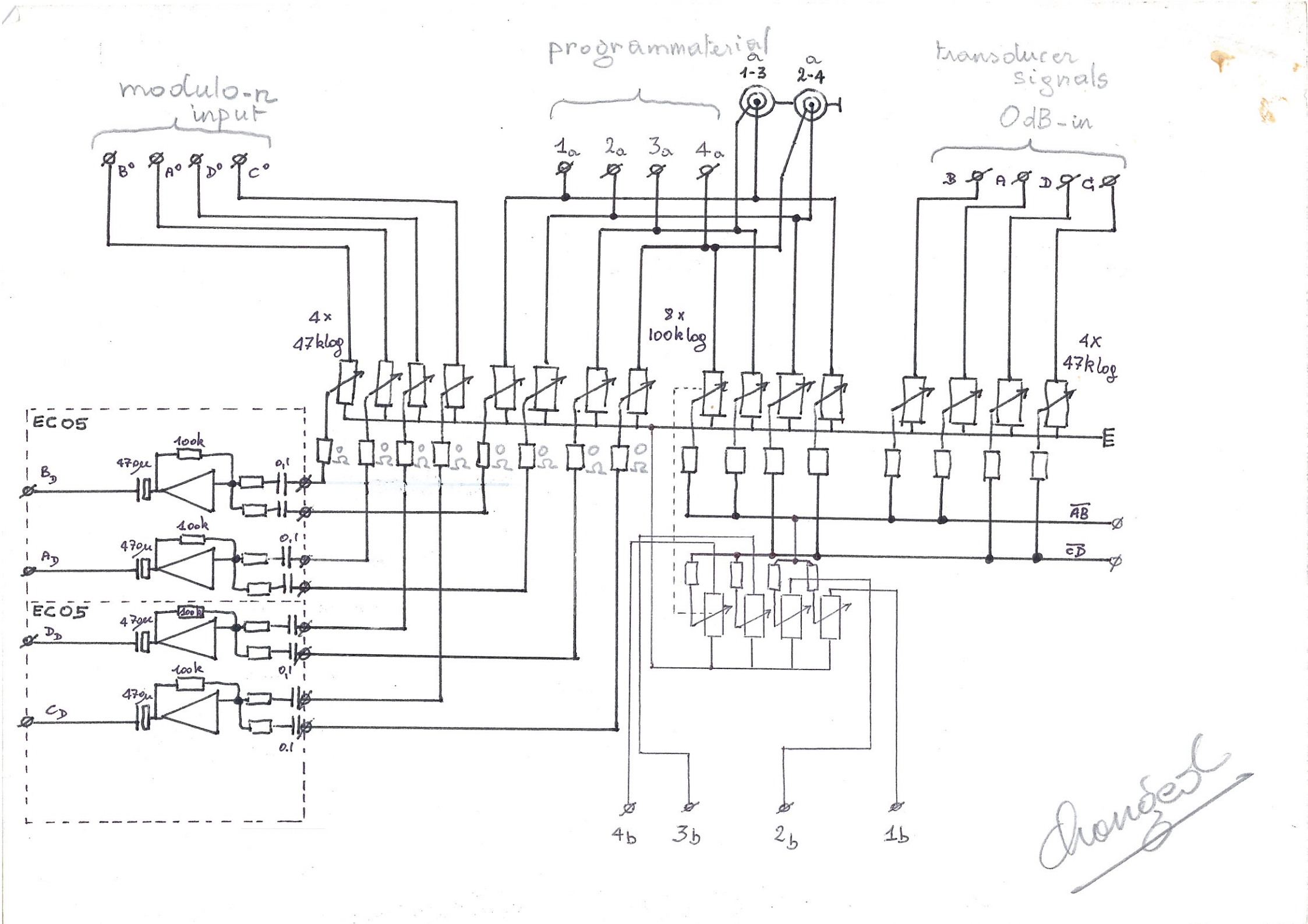




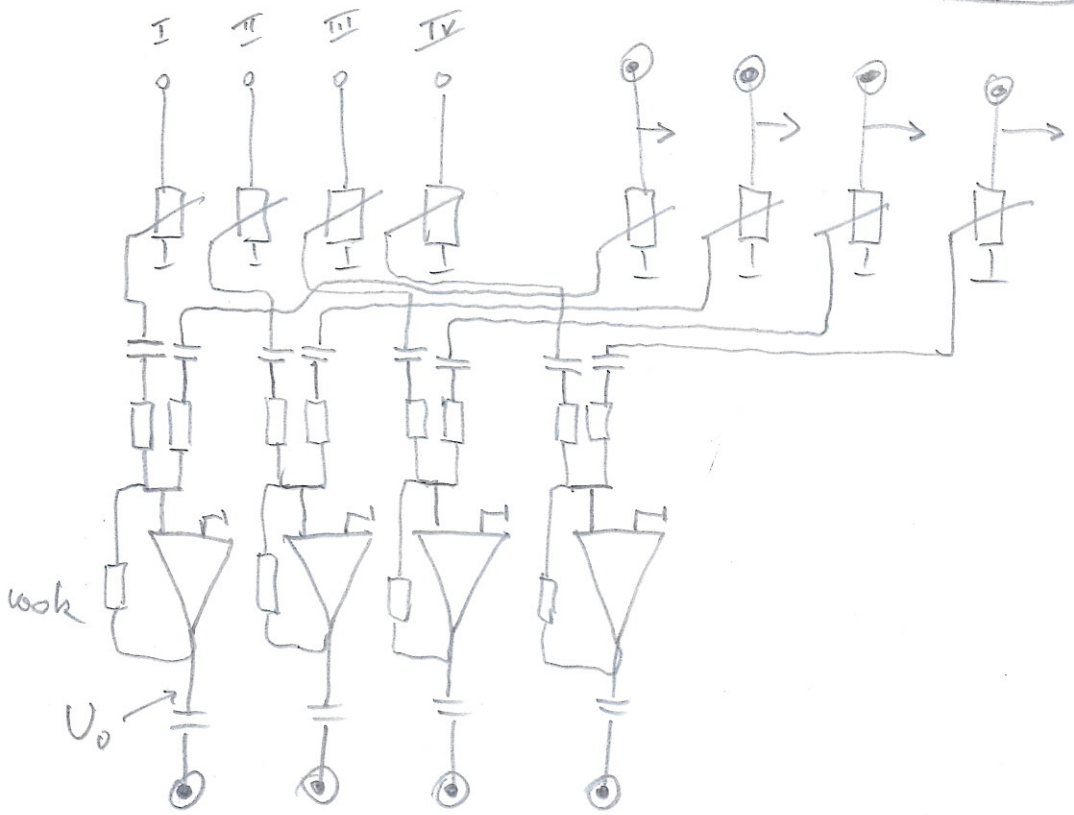







modulo-n input
programmateriel
transducer signals
0dB-in
a 1-3
a 2-4
1a 2a 3a 4a
B° A° D° C°
B A D C
4x 47klog
8x 100klog
4x 47klog
E
AB
CD
EC05
EC05
100k
47ou
0,1
4b 3b 2b 1b

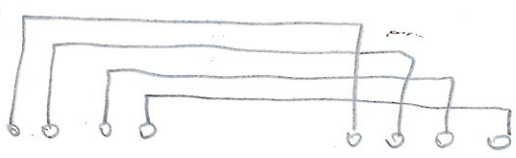
Berekening Mixer-print linkerdeel
(feedback-sturing)



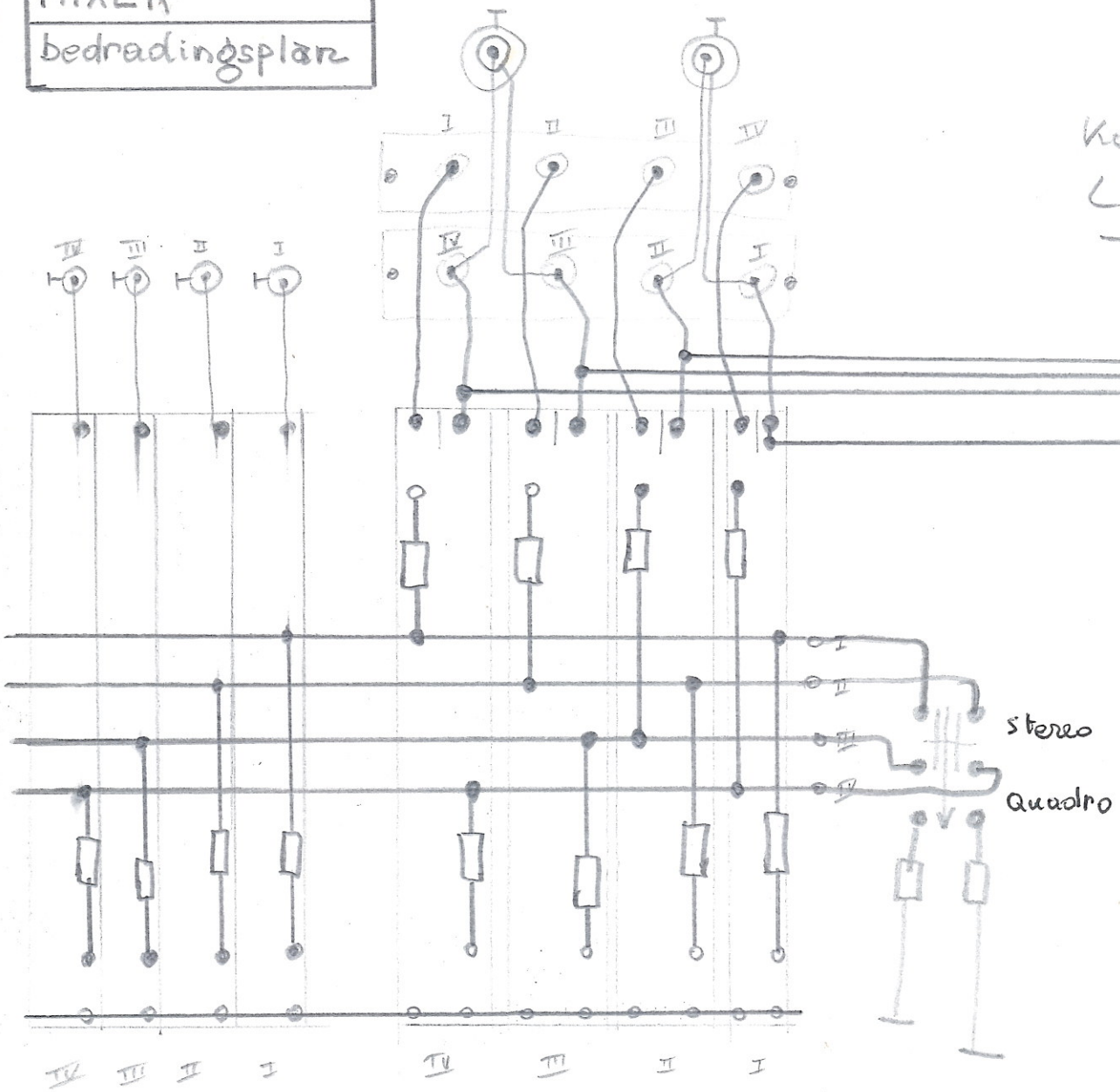
$$U_o = -10^5 \left(\frac{0{,}775}{10^5} + \frac{0{,}775}{10^5} \right)$$

$$= -10^5 \left(\frac{1{,}55}{10^5} \right) = = -1{,}55\,V$$

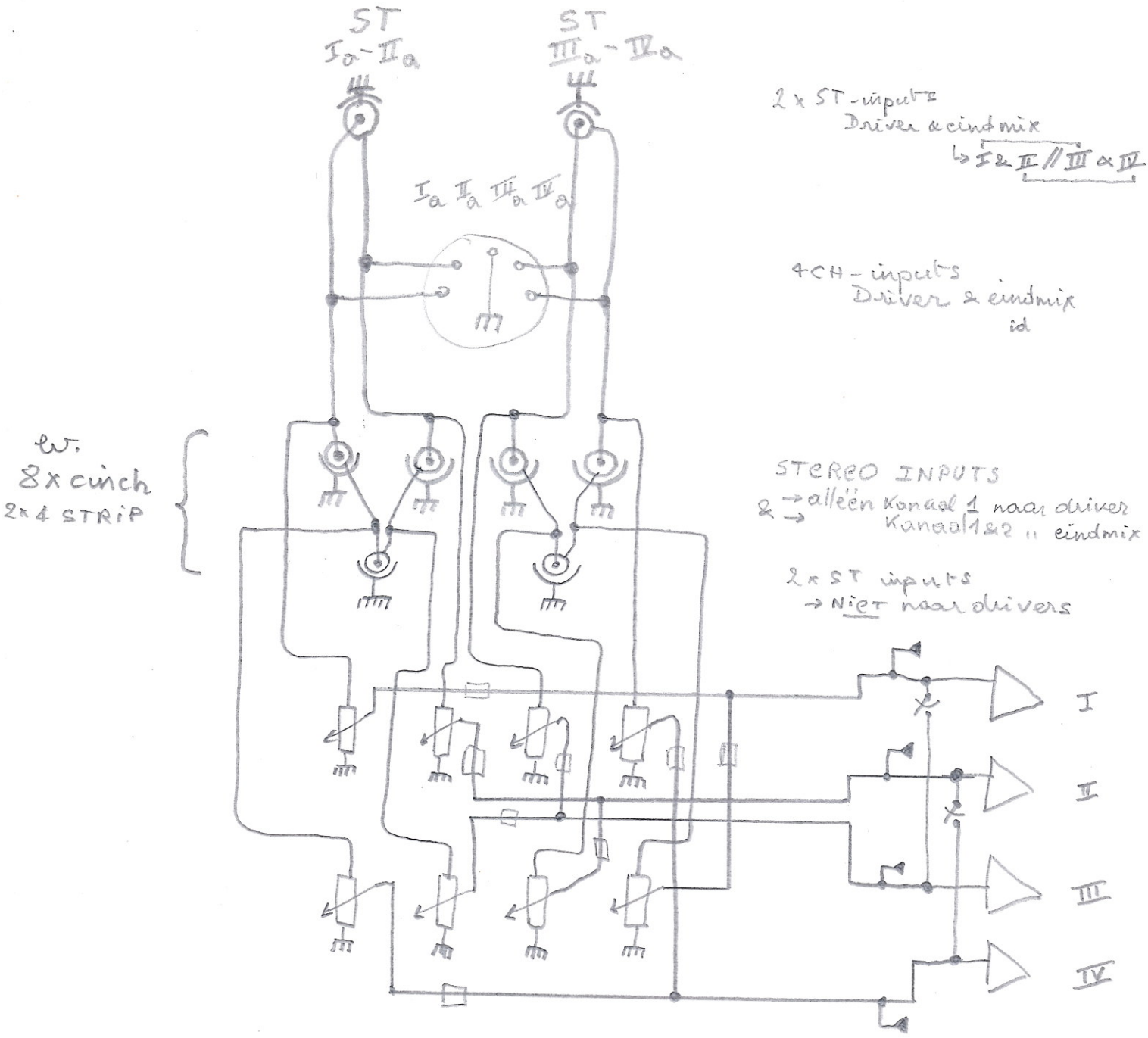
mixbekerdeel

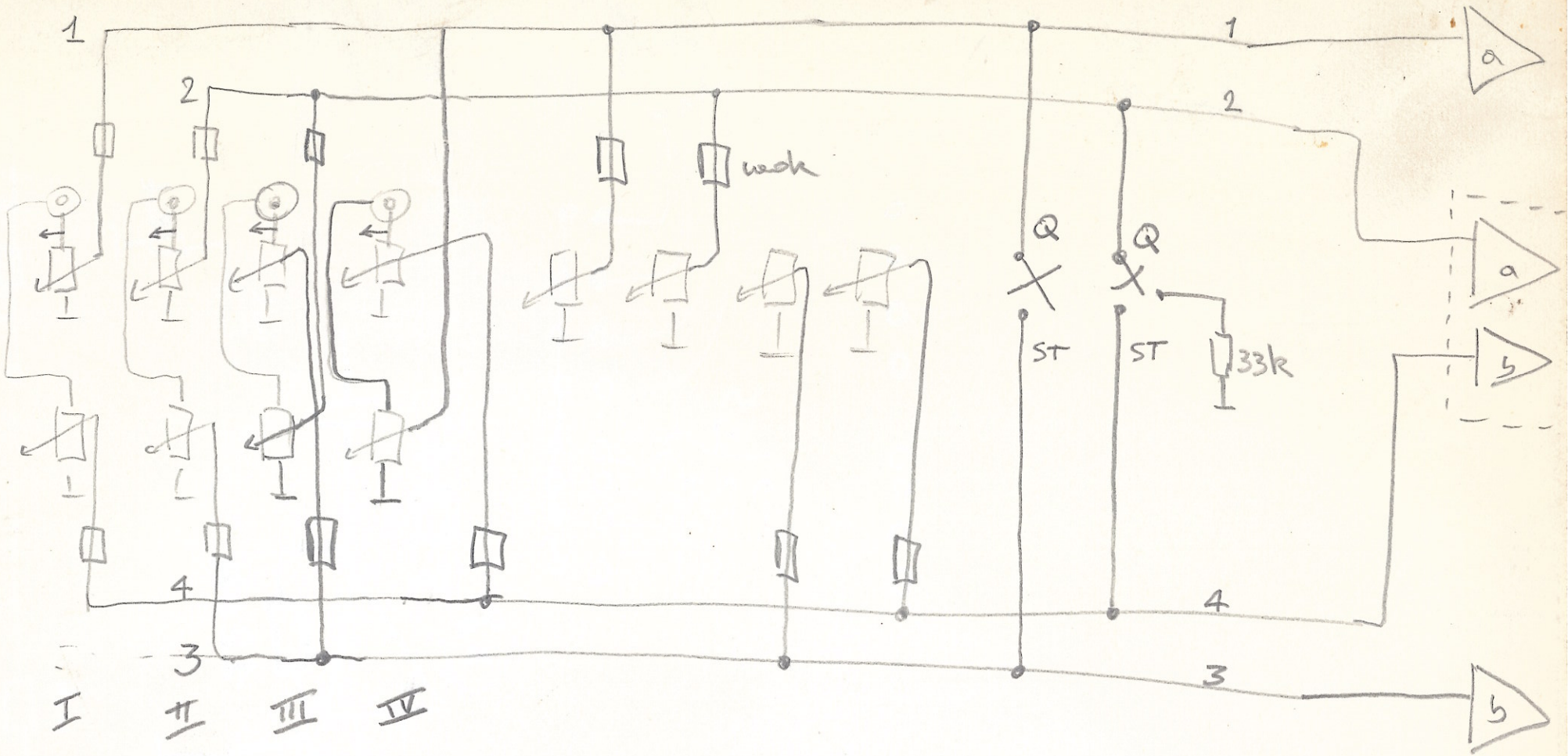


MIXER
bedradingsplan



Koppensjoe
Links.


ST
Ia - IIa
ST
IIIa - IVa
Ia IIa IIIa IVa
2 x ST-inputs
Driver & eindmix
↳ I & II // III & IV
4CH-inputs
Driver & eindmix
id
ev.
8x cinch
2x4 STRIP
STEREO INPUTS
& → alleen Kanaal 1 naar driver
Kanaal 1&2 → eindmix
2x ST inputs
→ Niet naar drivers
I
II
III
IV

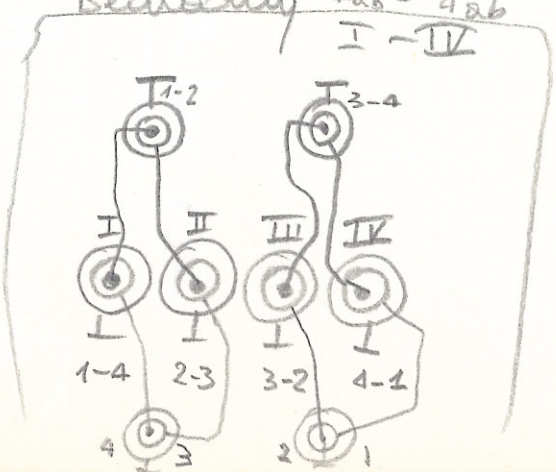


I = 1 & 4 → ST

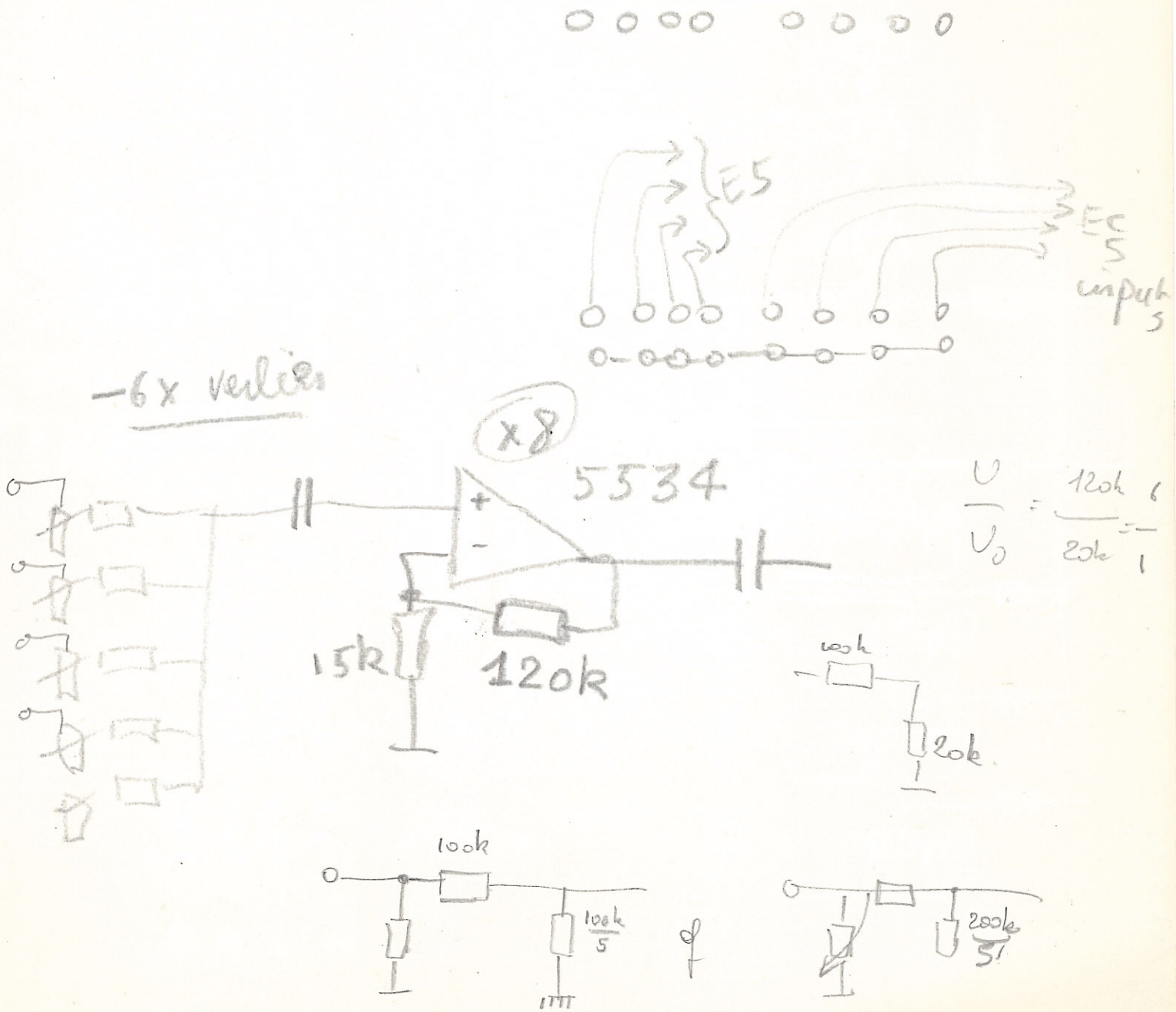
II = 2 & 3 → ST

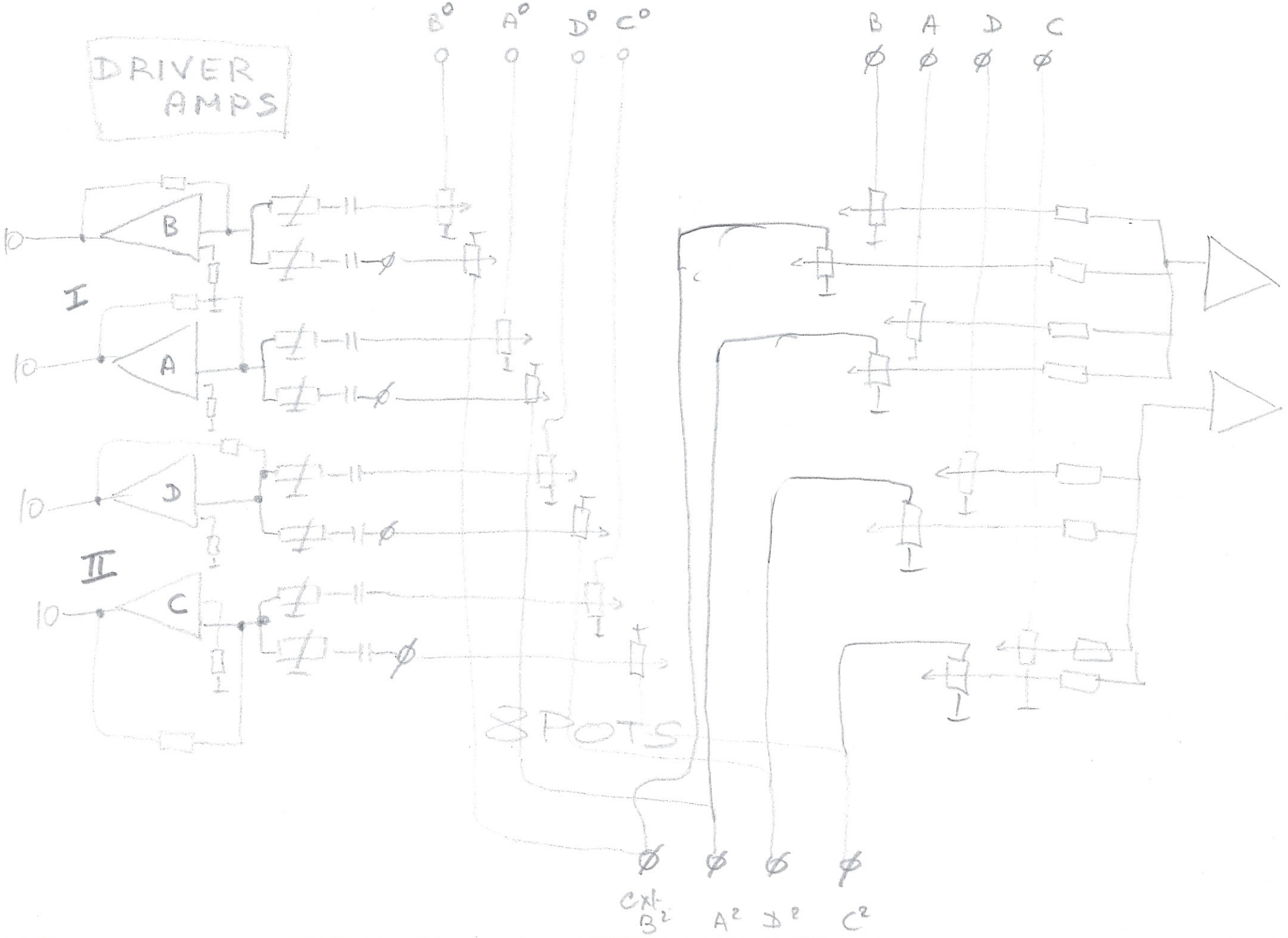
III = 3 & 2 → ST

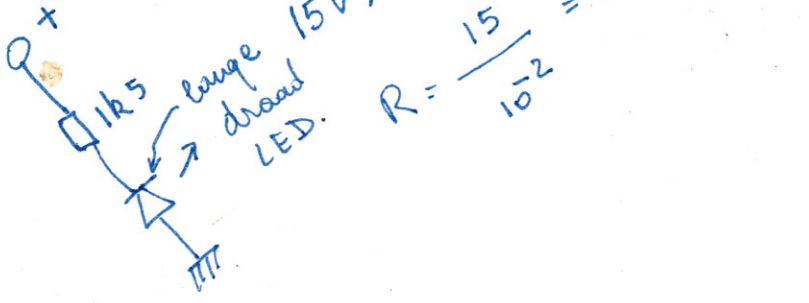
IV = 4 x 1

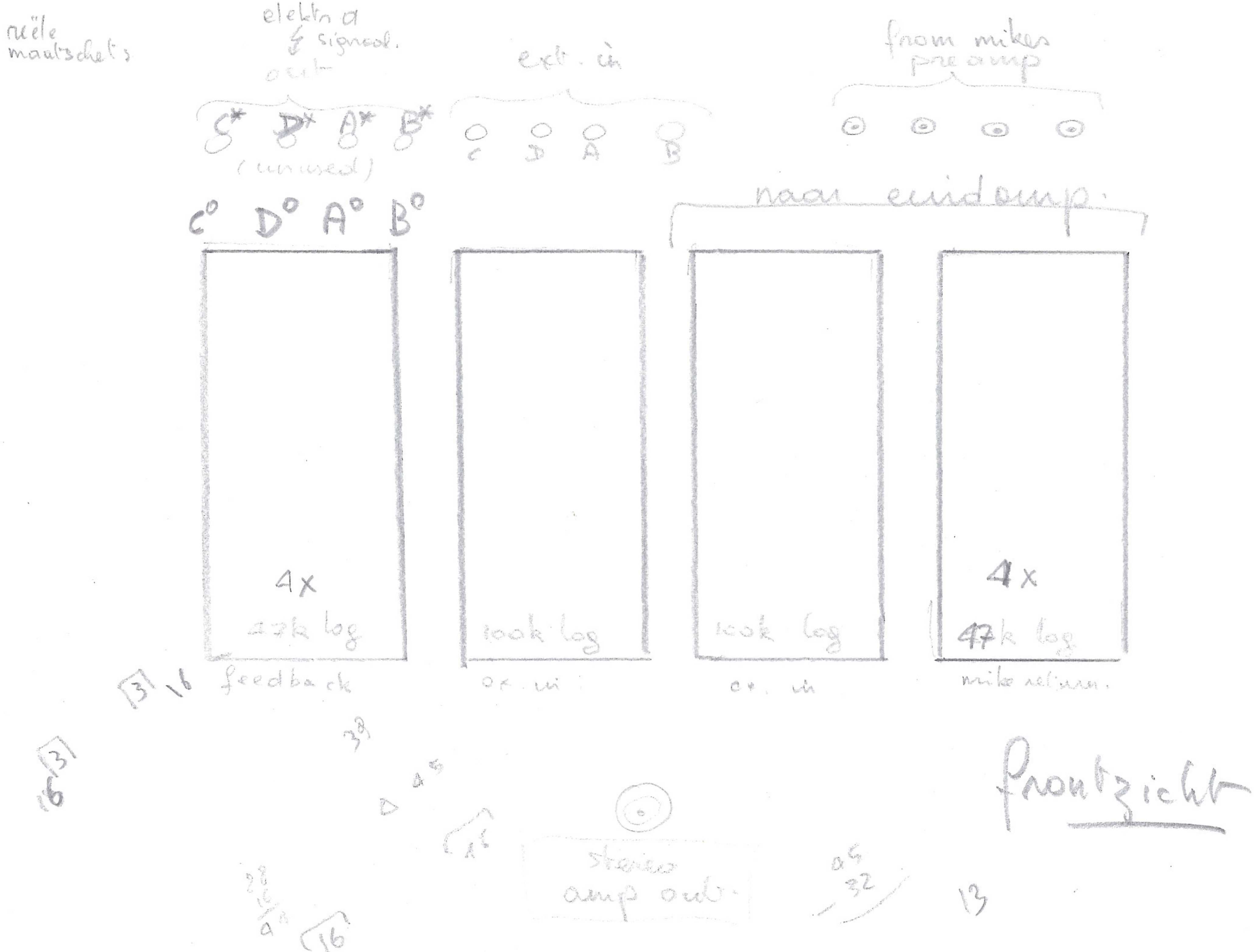


Rechterdeel
MIXER


ES
ES
5
inputs
-6x vedle
x8
5534
15k
120k
100k
20k
100k
100k
5
200k
5

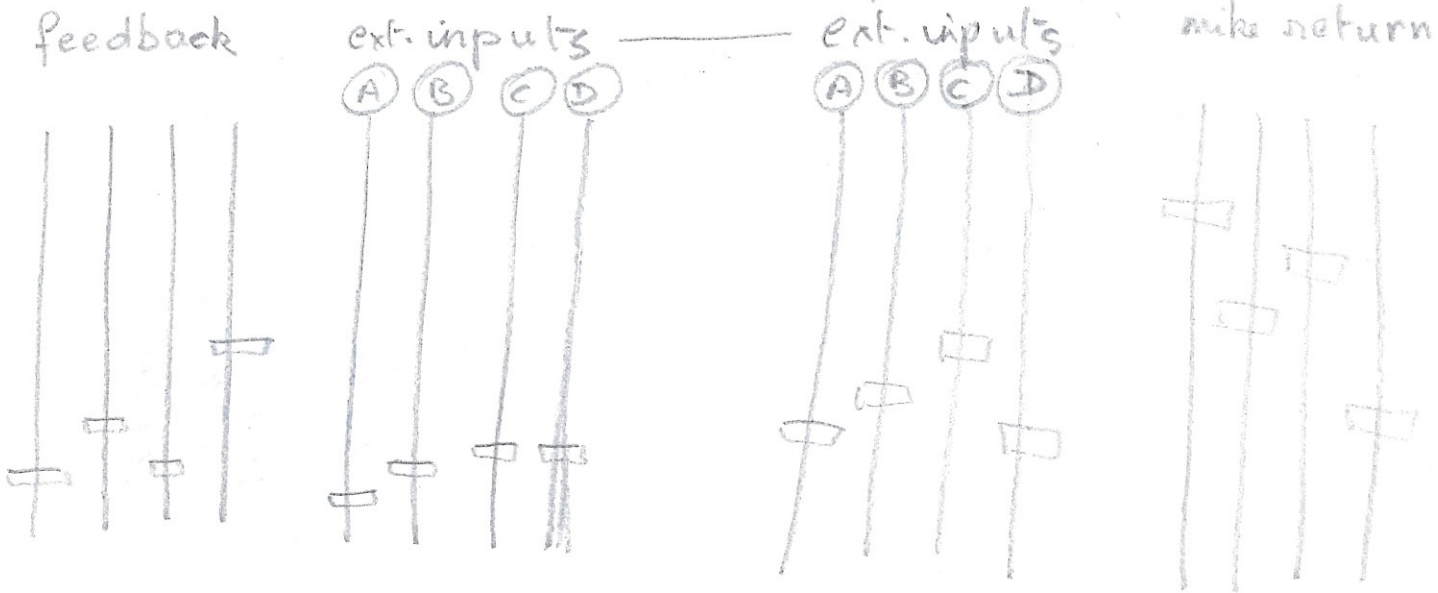

DRIVER AMPS
B°
A°
D°
C°
B
A
D
C
I
II
10
8 POTS
CXL. B²
A²
D²
C²

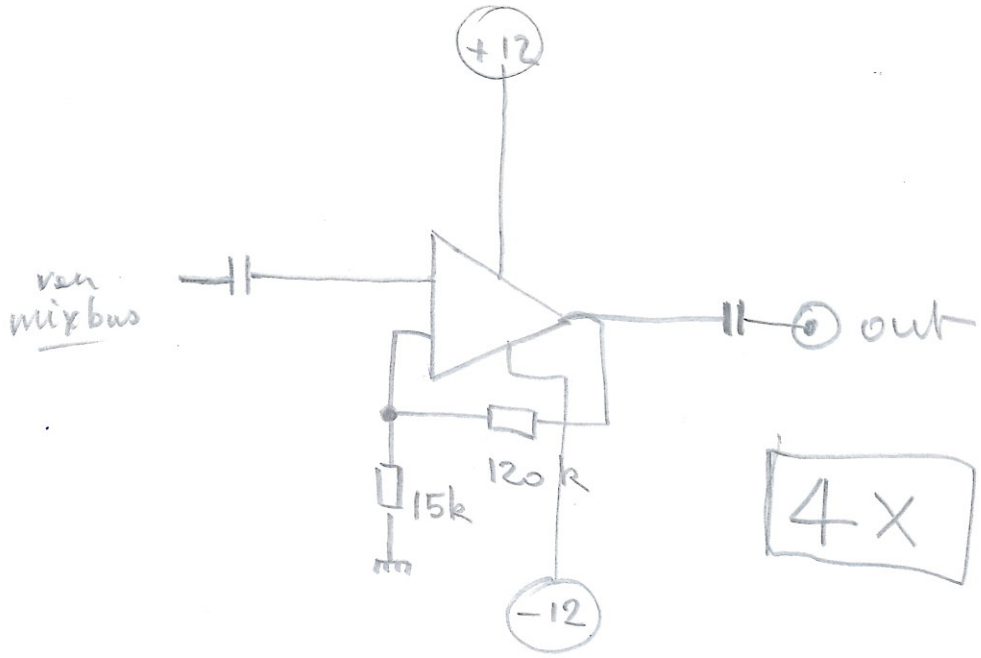

+
1k5
large
droad
LED.
15V / 0,01A
$R = \frac{15}{10^{-2}} = 15.10^2 = 1k5$



reële maatschets
elektra & signaal out
C* D* A* B*
(unused)
ext. in
C D A B
from mikes preamp
naar eindamp.
C° D° A° B°
4x
47k log
100k log
100k log
4x
47k log
feedback
ex. in
ex. in
mike return.
stereo amp out.
frontzicht
13

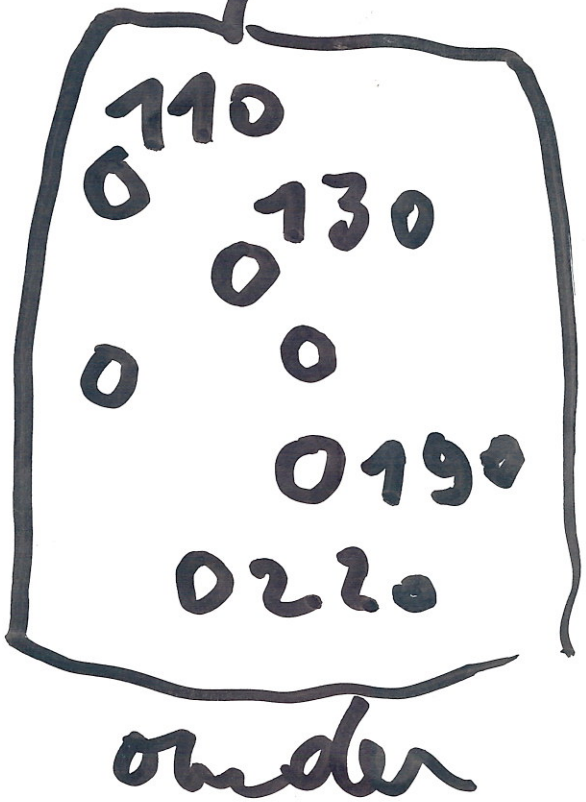
DRIVER
MIX

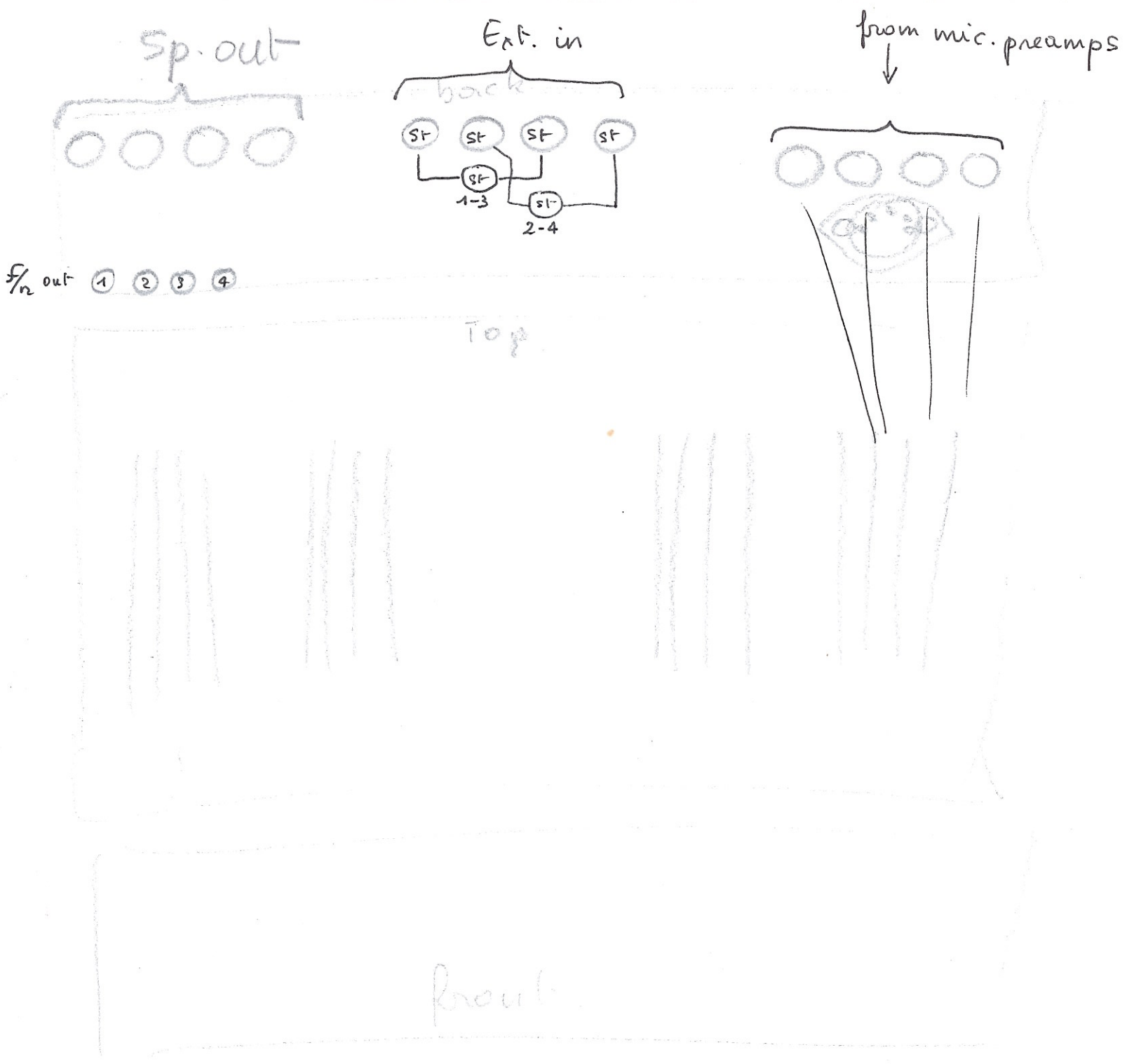


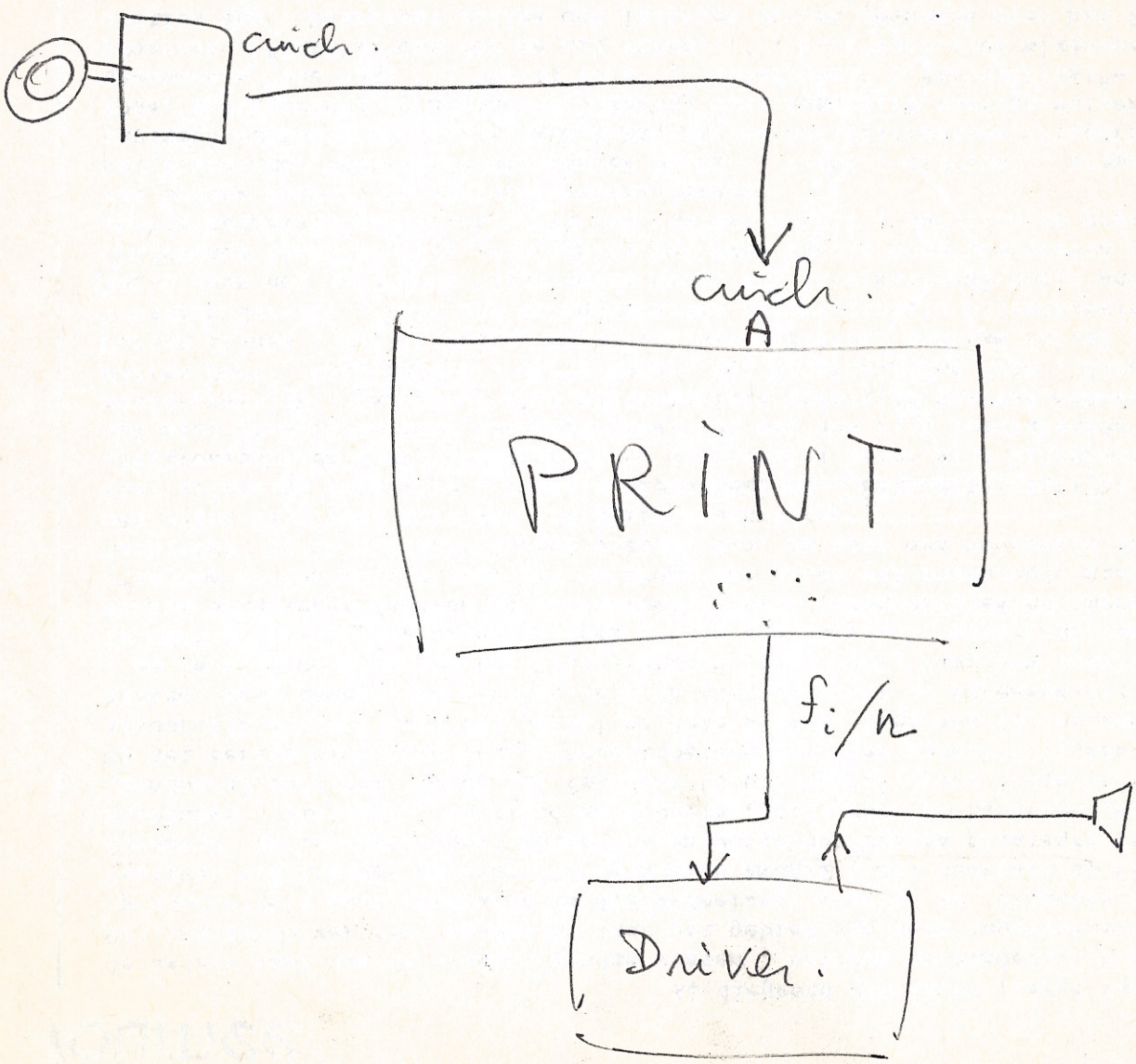


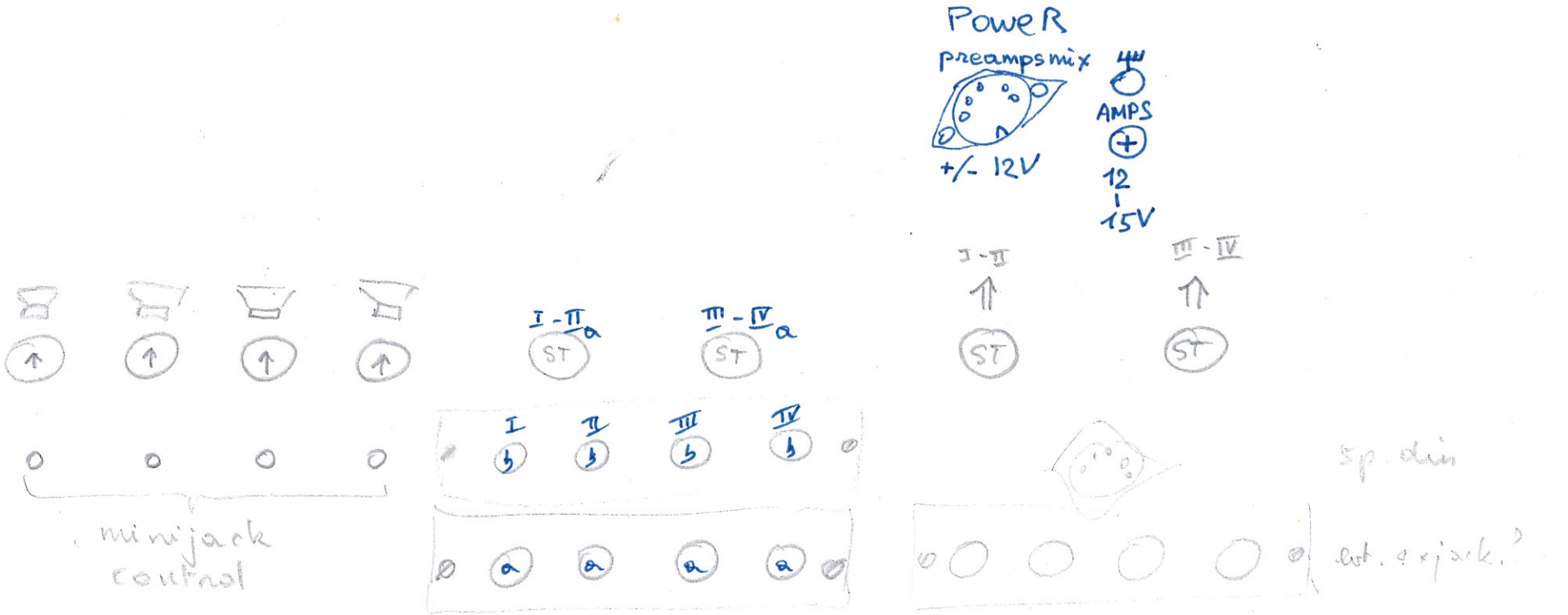
×8 amp

100k - met film 30x


110
130
190
220
onder


Sp. out
Ext. in
back
St
St
St
St
St
1-3
St
2-4
from mic. preamps
f/n out 1 2 3 4
Top
front


anch.
anch.
A
PRINT
fi/n
Driver.

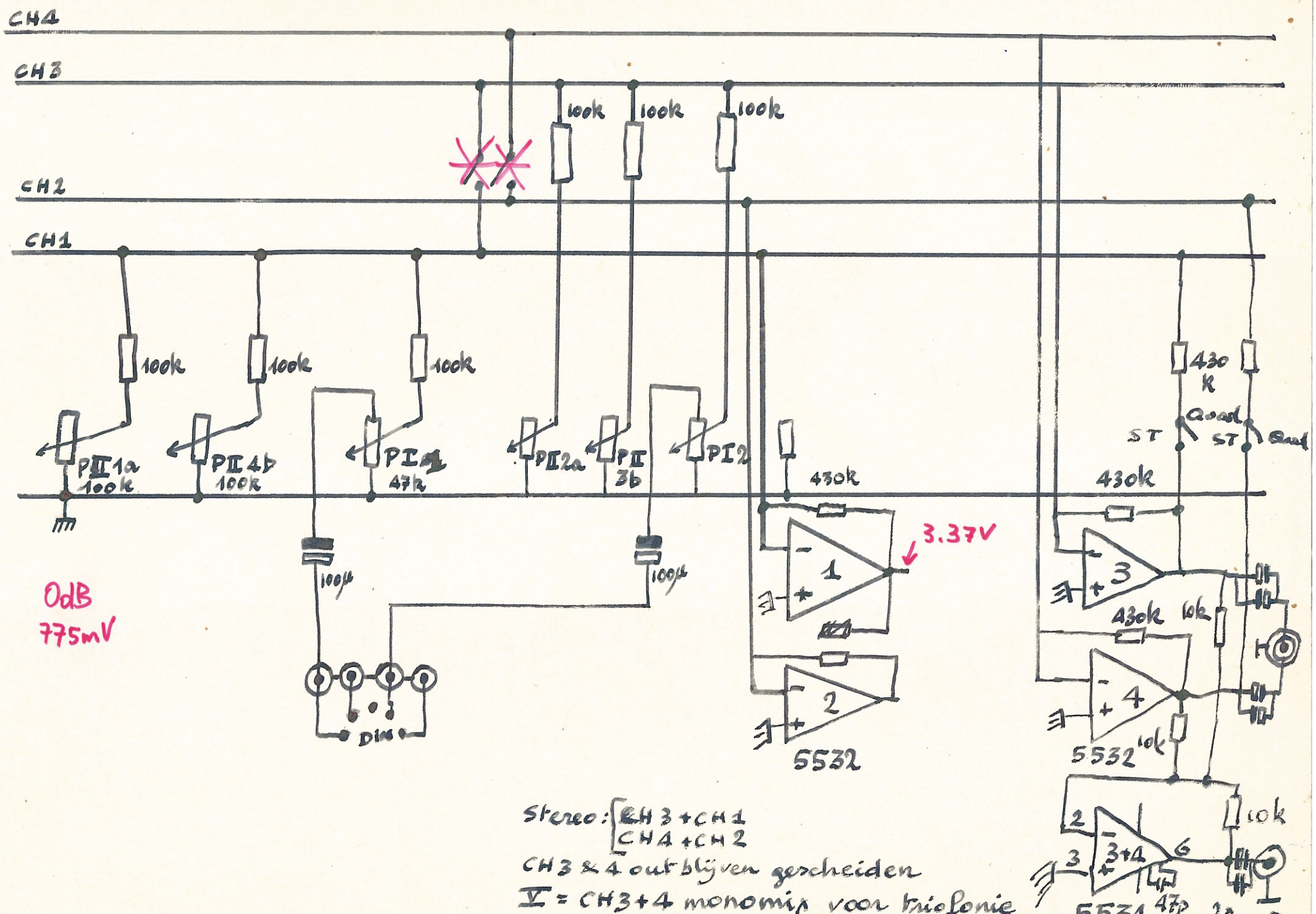


$$\frac{10^{6}}{23} \qquad 25.000 \cdot 10^{-9}$$

$$100pF = 40k \qquad 25.10^{-6}$$

$$Zc = \frac{1}{2\pi f c}$$

$$6,29 \cdot 40.10^{3} \cdot 100.10^{-12}$$

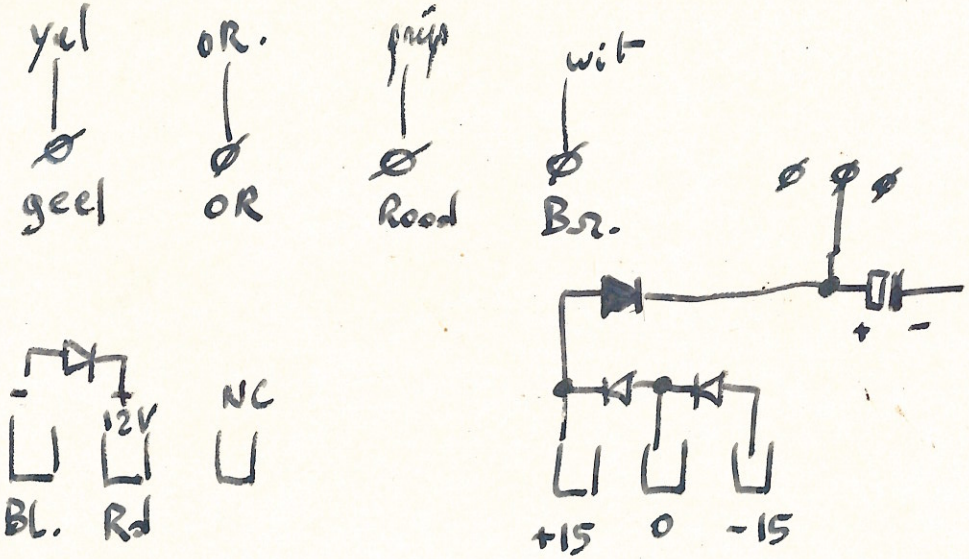


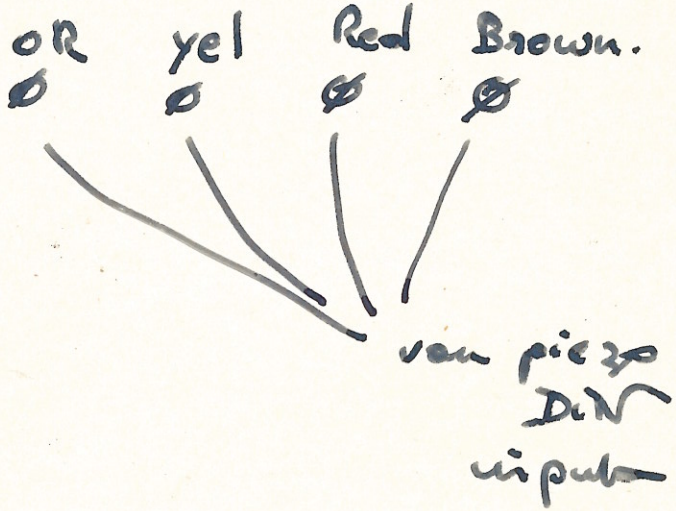
Stereo: { CH3 + CH1 / CH4 + CH2

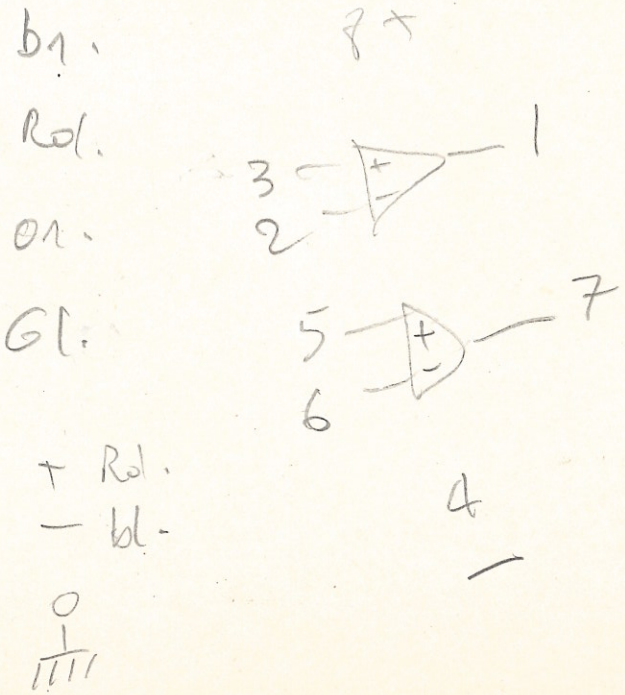
CH3 & 4 out blijven gescheiden

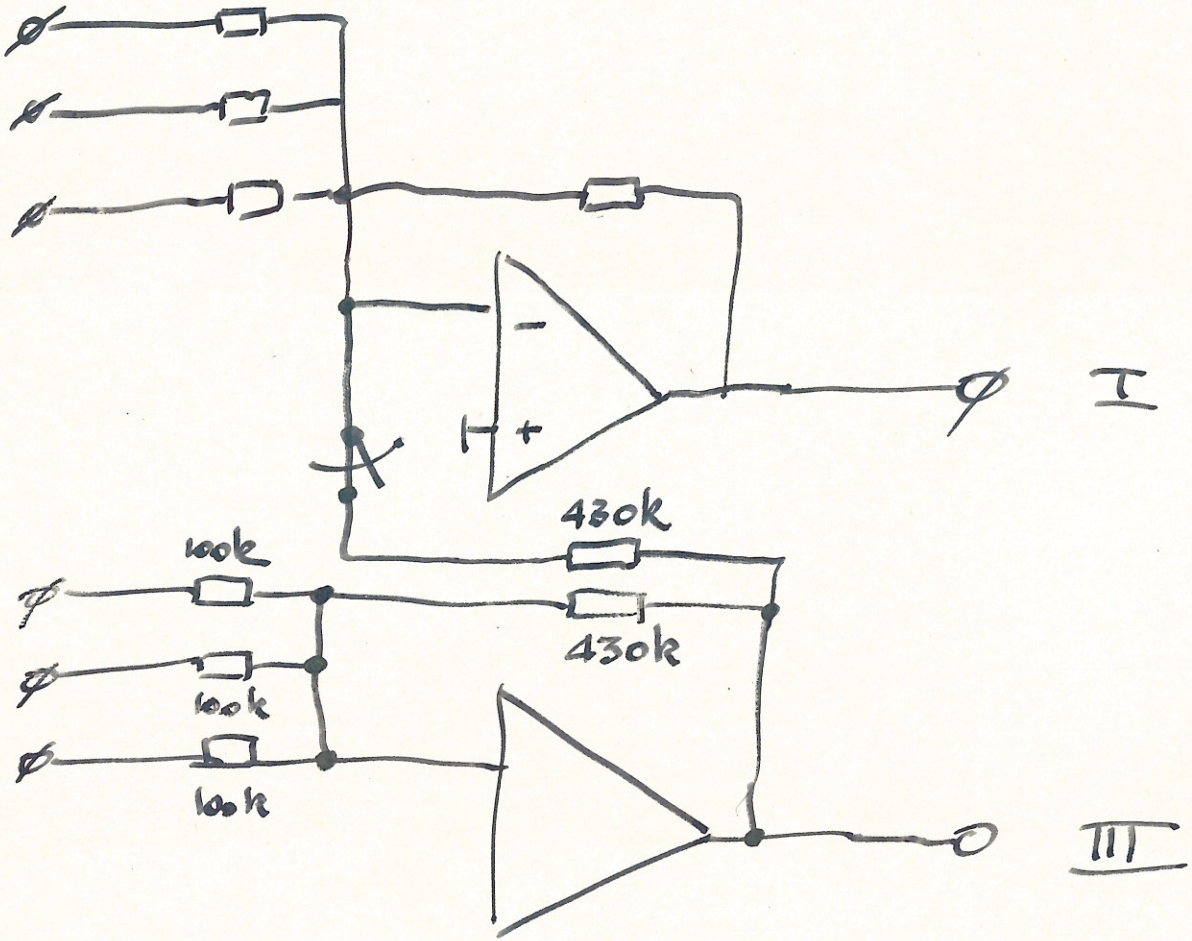
V = CH3+4 monomix voor triofonie

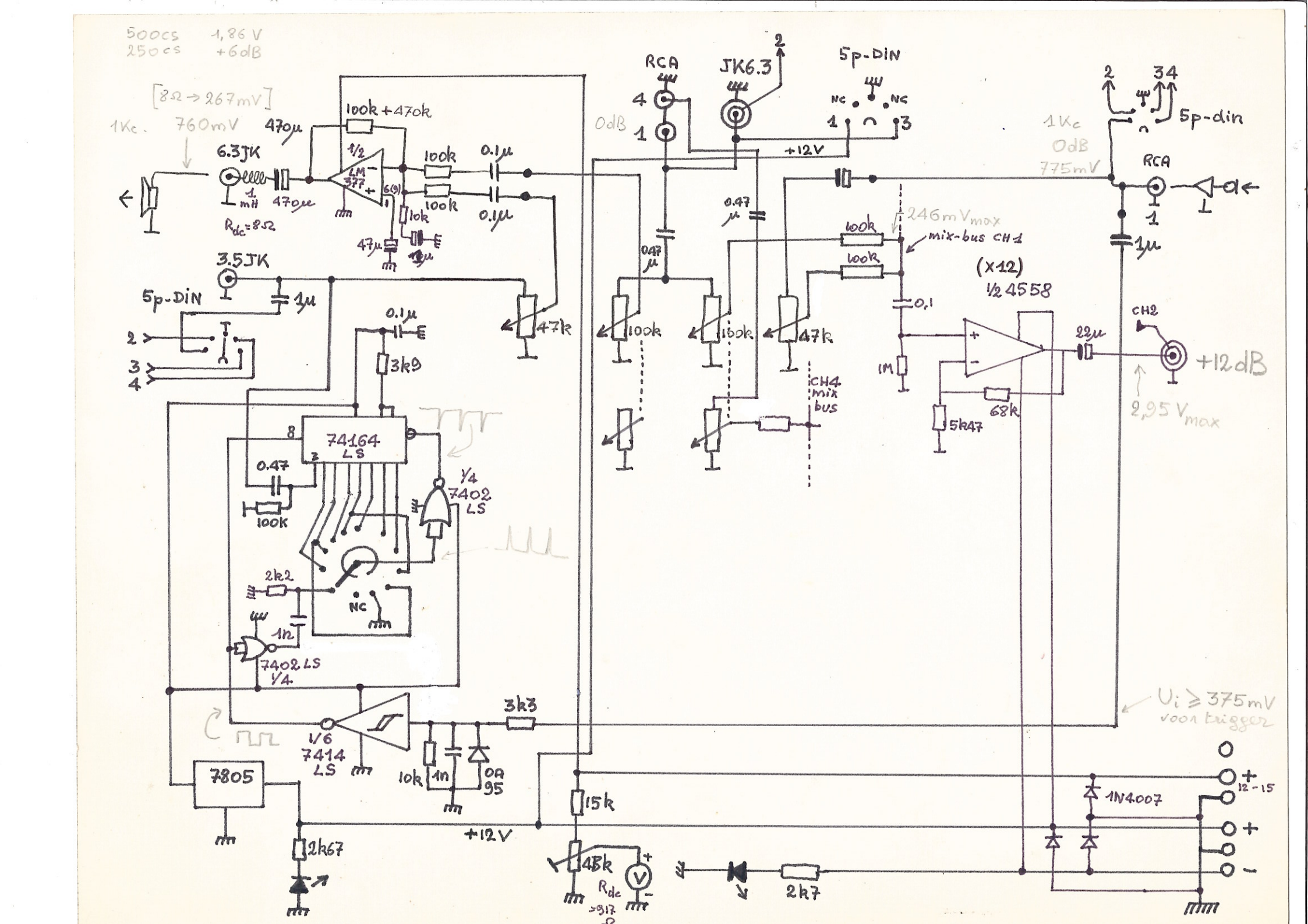
Demontage N.S.U. sound mixer 11/1986

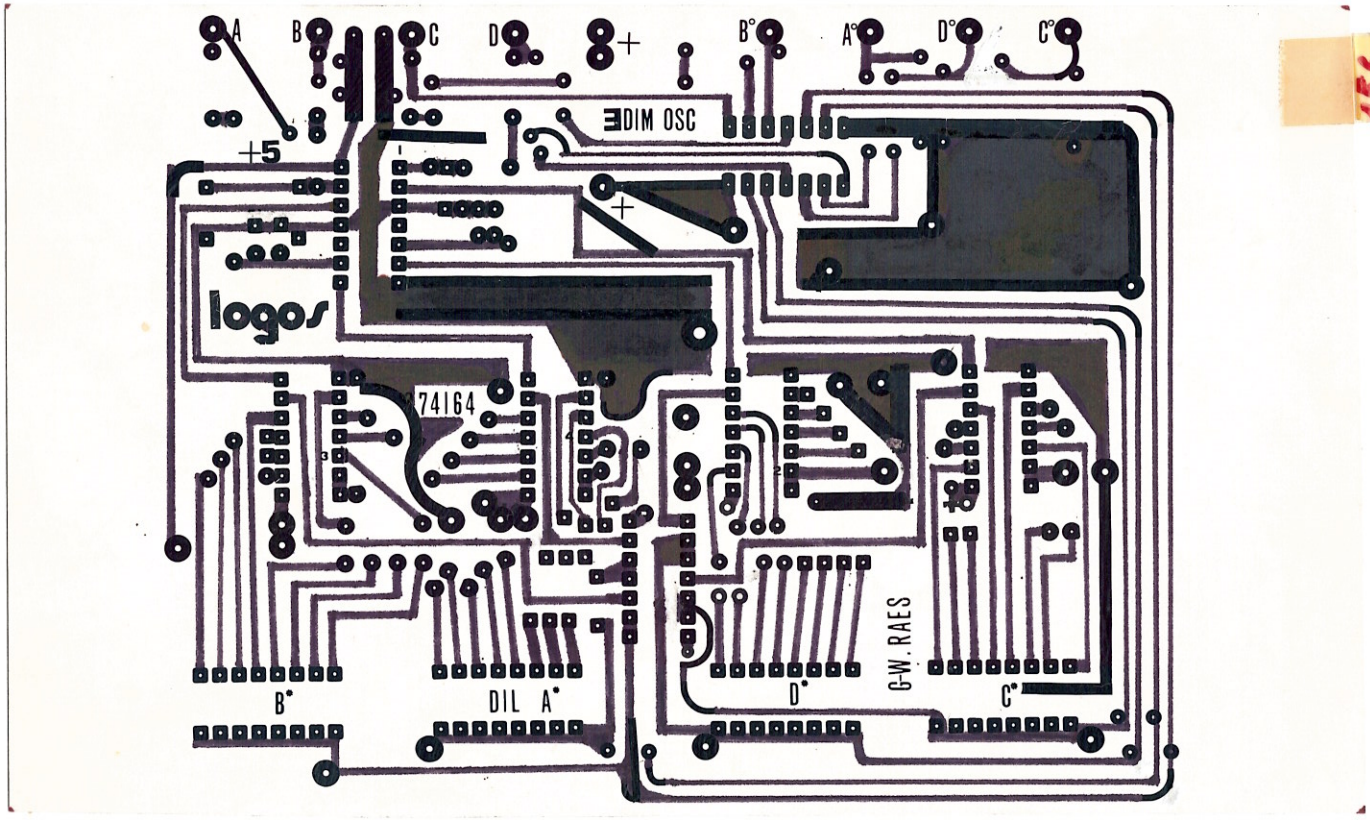


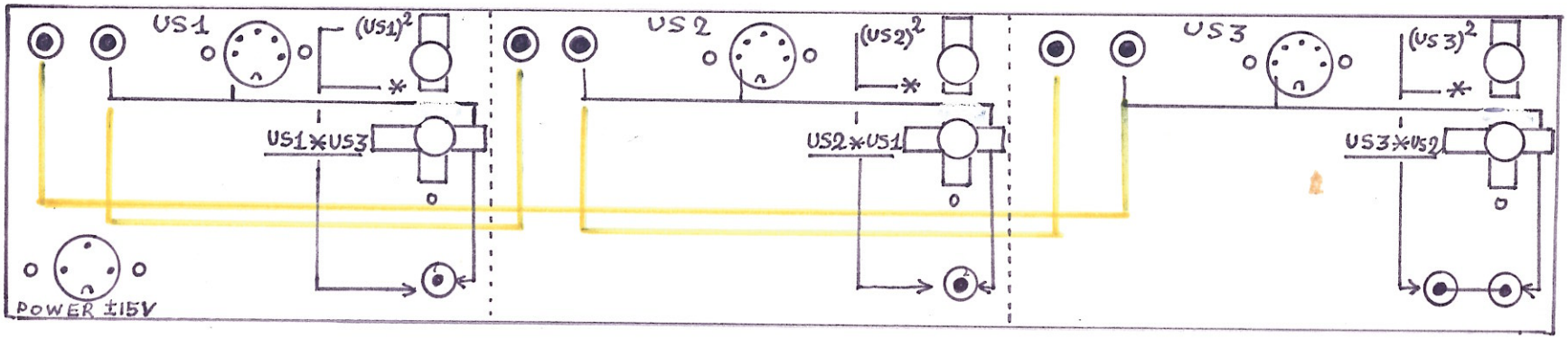





100k
430k
430k
100k
100k
I
II


500cs 1,86 V
250cs +6dB
[8Ω → 267mV]
1Kc. 760mV
6.3JK
1 mH
470µ
Rdc=8Ω
100k+470k
1/2 LM 377
100k
0.1µ
10k
47µ
3.5JK
5p-DIN
1µ
47k
3k9
74164 LS
0.47
100K
1/4 7402 LS
2k2
NC
1n
7402 LS 1/4
1/6 7414 LS
3k3
10k
1n
OA 95
7805
2k67
+12V
15k
4Bk
Rdc =917
2k7
RCA
JK6.3
5p-DIN
0dB
+12V
0.47µ
100k
150k
47k
CH4 mix bus
246mV max
mix-bus CH4
(X12)
1/2 4558
0,1
1M
68k
5k47
22µ
CH2
+12dB
2,95 V max
1Kc
0dB
775mV
5p-din
1µ
Ui ≥ 375mV
voor trigger
1N4007
12-15


A
B
C
D
+
B°
A°
D°
C°
+5
3DIM OSC
logos
74164
B°
DIL A°
D°
C°
G-W. RAES


US1
(US1)²
US1*US3
US2
(US2)²
US2*US1
US3
(US3)²
US3*US2
POWER ±15V

17/12/84 PCR.
Polis
456583
1272

1 VA / 8 Ω

V?

$$1\,VA \cdot 8\frac{V}{A}$$

$$= 8\,V^2$$

$$V = \sqrt{8}$$

Voor 1Watt out

moet U_{out} = 2,83 Volt — $8V_{pp}$.

2Watt

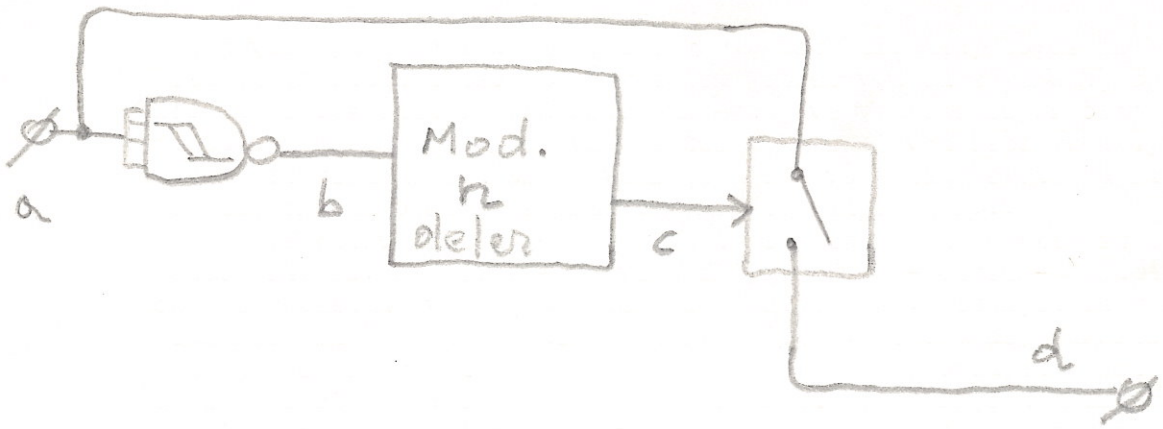
U_{out} = 4 Volt — $11,3V_{pp}$

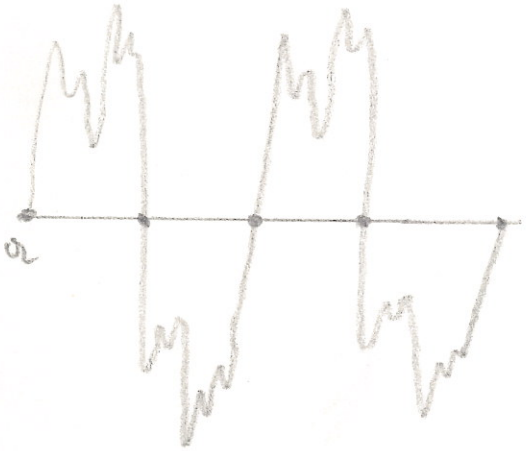
3 Watt

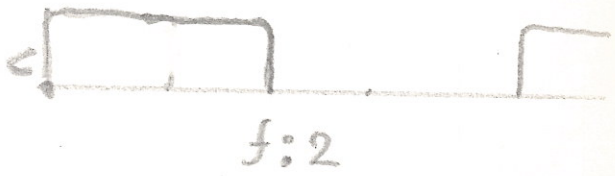
U_{out} = 4,9 Volt — $13,8V_{pp}$

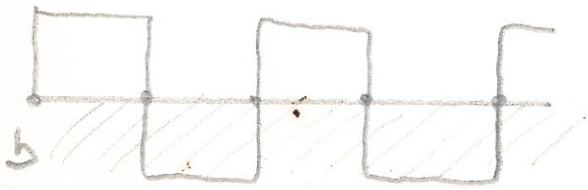
4 Watt

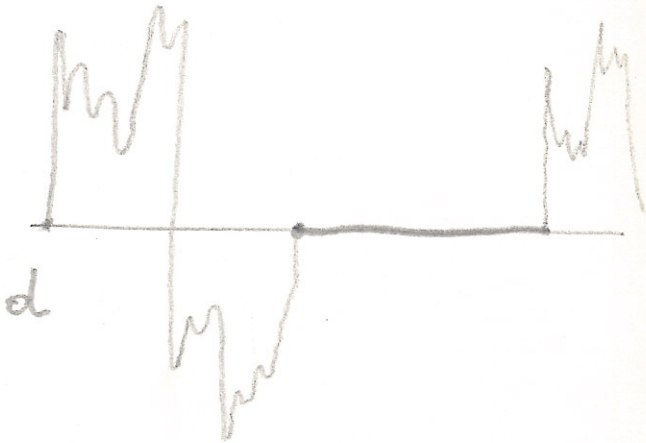
U_{out} = 5,6 Volt — 15


Mod.
n
oleler
a
b
c
d

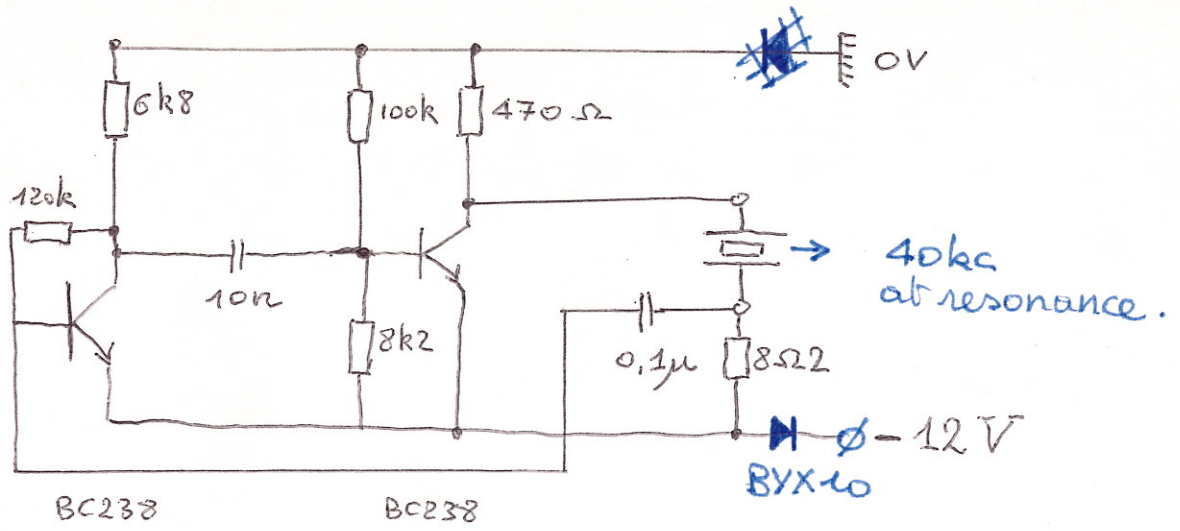

a


c
f:2

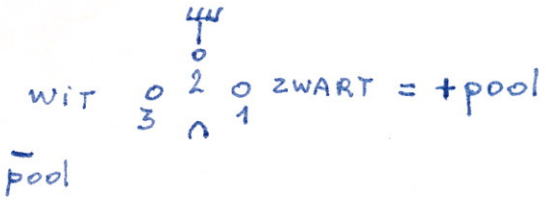

b


d

ZENDER-II ULTRASOON PROJEKT



output pressure: ca. 0,5 Pa
at 1 meter



$$I_{cmax} = \frac{15}{470} = 30mA$$

(bij 15V)

bij 9V : 20mA max.

15
00
150
1500

470
0,03

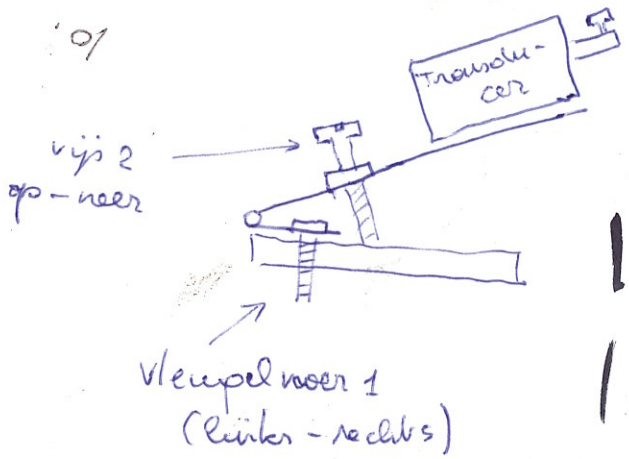
9
0
90
900

470
0,02

13mA
US-3
US-2

US1:
8mA

117
104



120mA 15V
-15mA

37mA/KV
à 120mA

Tabak schaadt de gezondheid
Le tabac nuit à la santé
Tabak schädigt die Gesundheit
A.R. K.B. 30.3.81 F.95

13
13
8
34

120
34
86

Juan Hidalgo

Walter Marchetti

Viale

Battistelli, Georgio

(Rond) (percussion)

Zossi

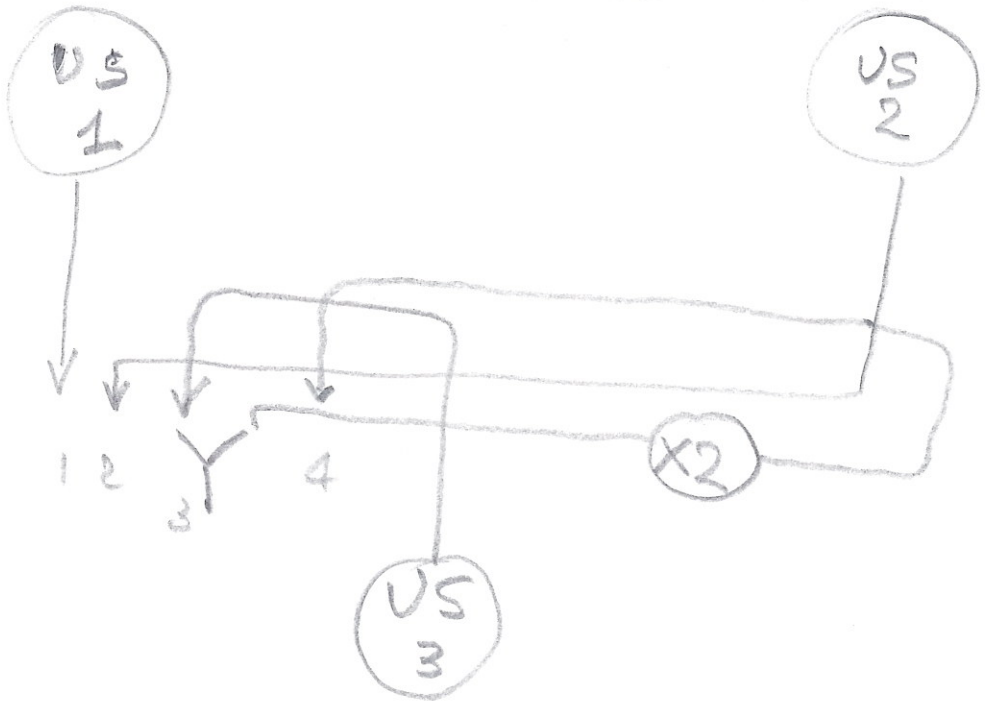
Condini
1 ~~wit~~
3 ~~wit~~ zwart
2 massa

Hältinger Linz

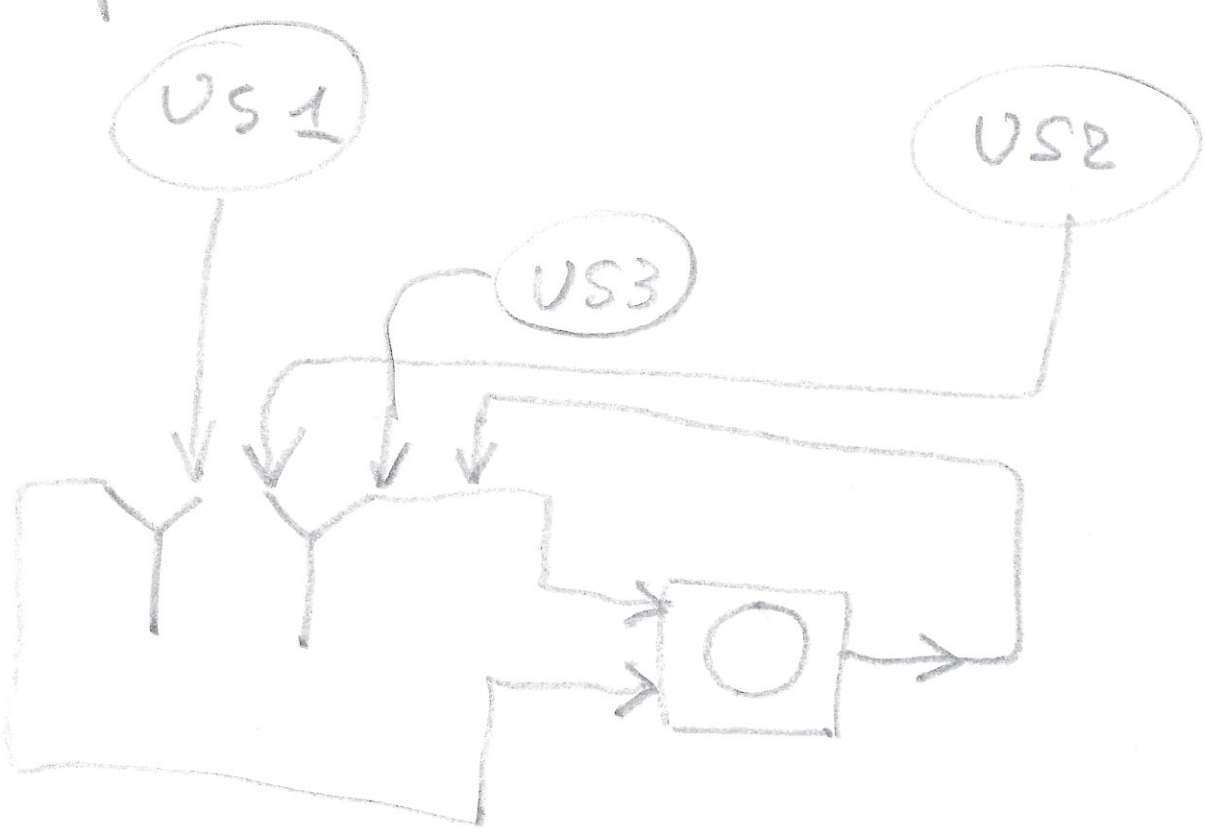
Ars Electronica

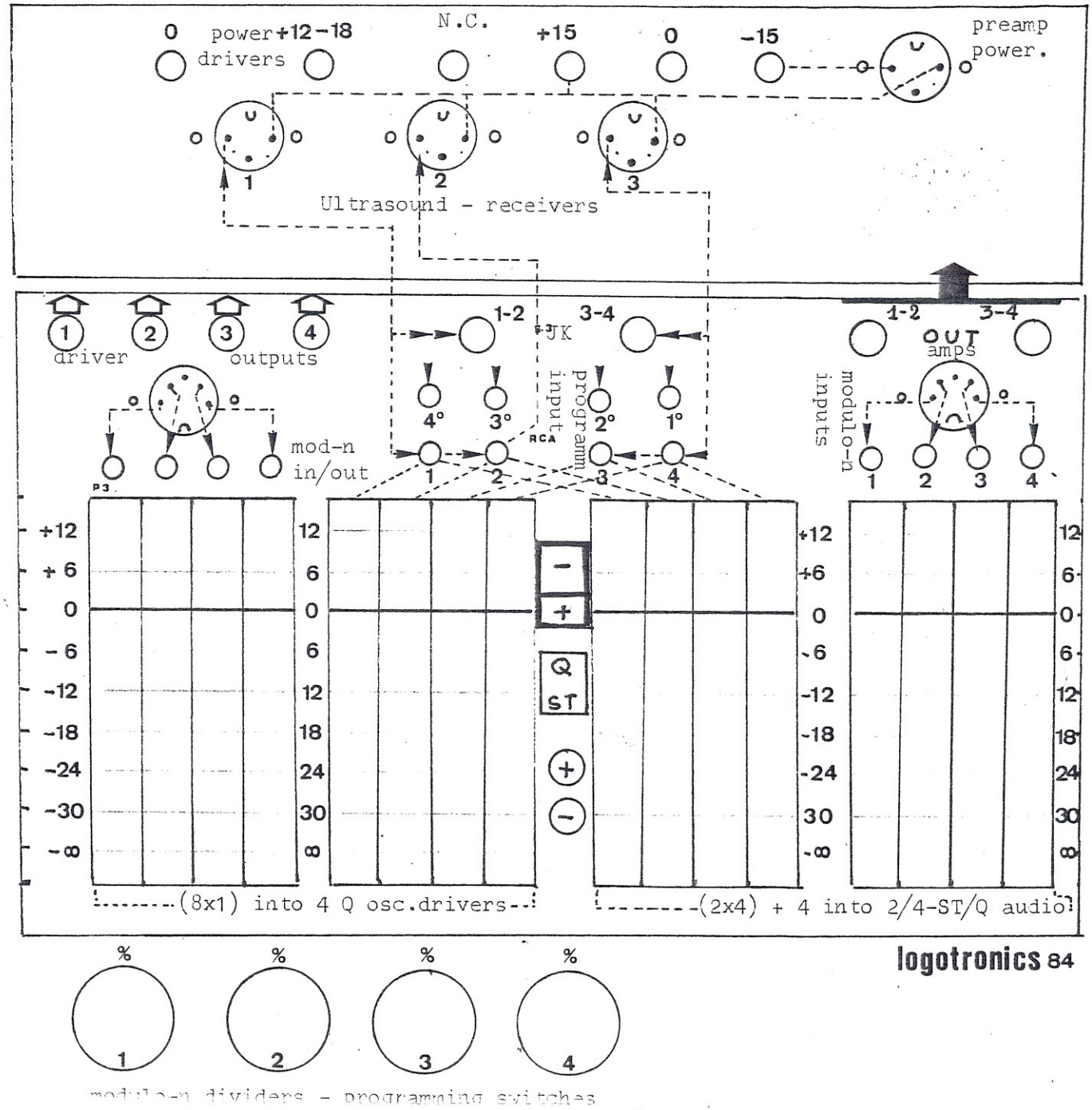
5polig: 1=
3=wit 1=rood

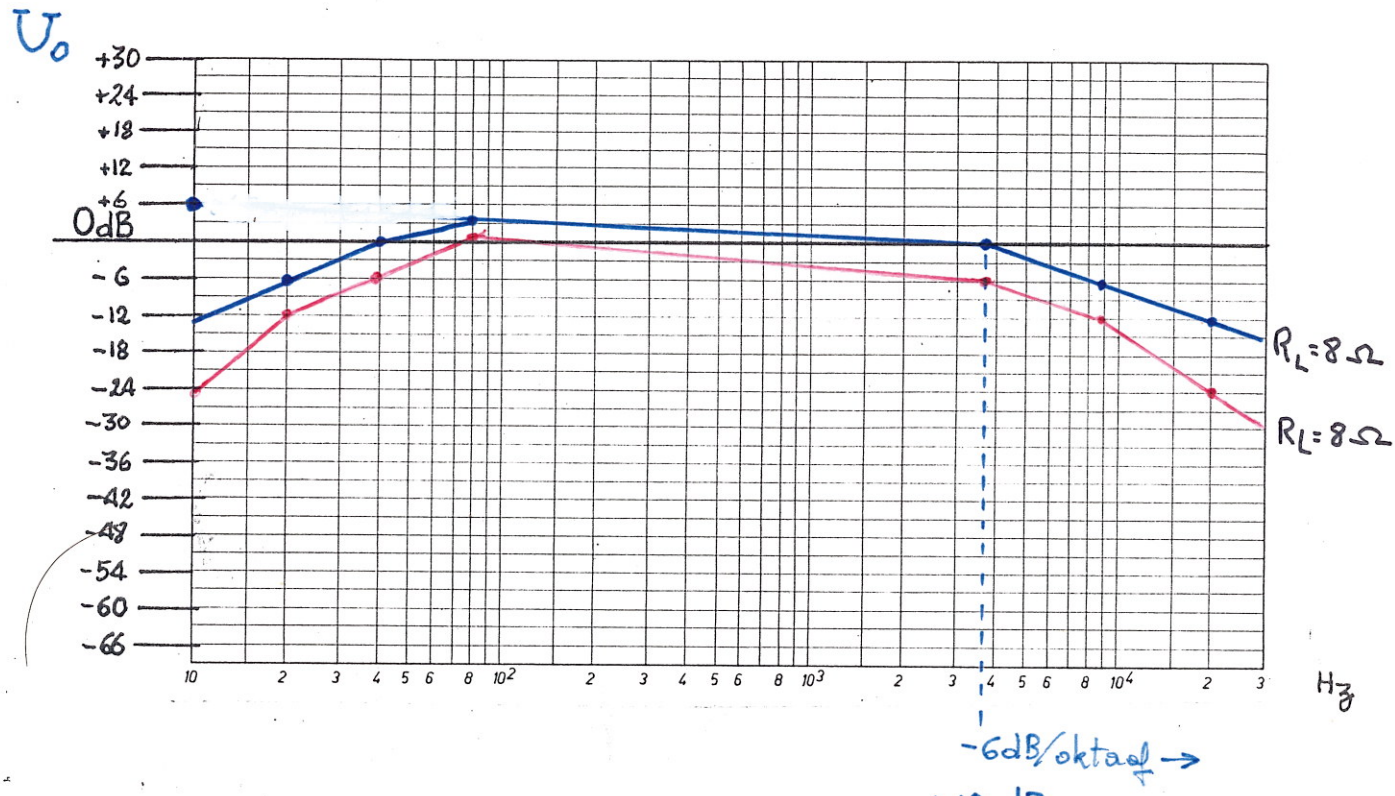
Patches

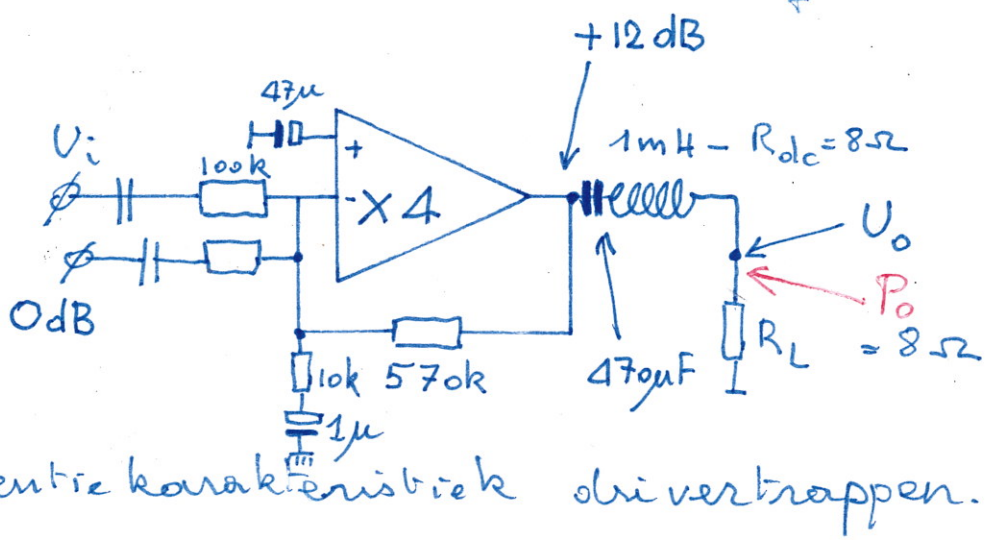


f.

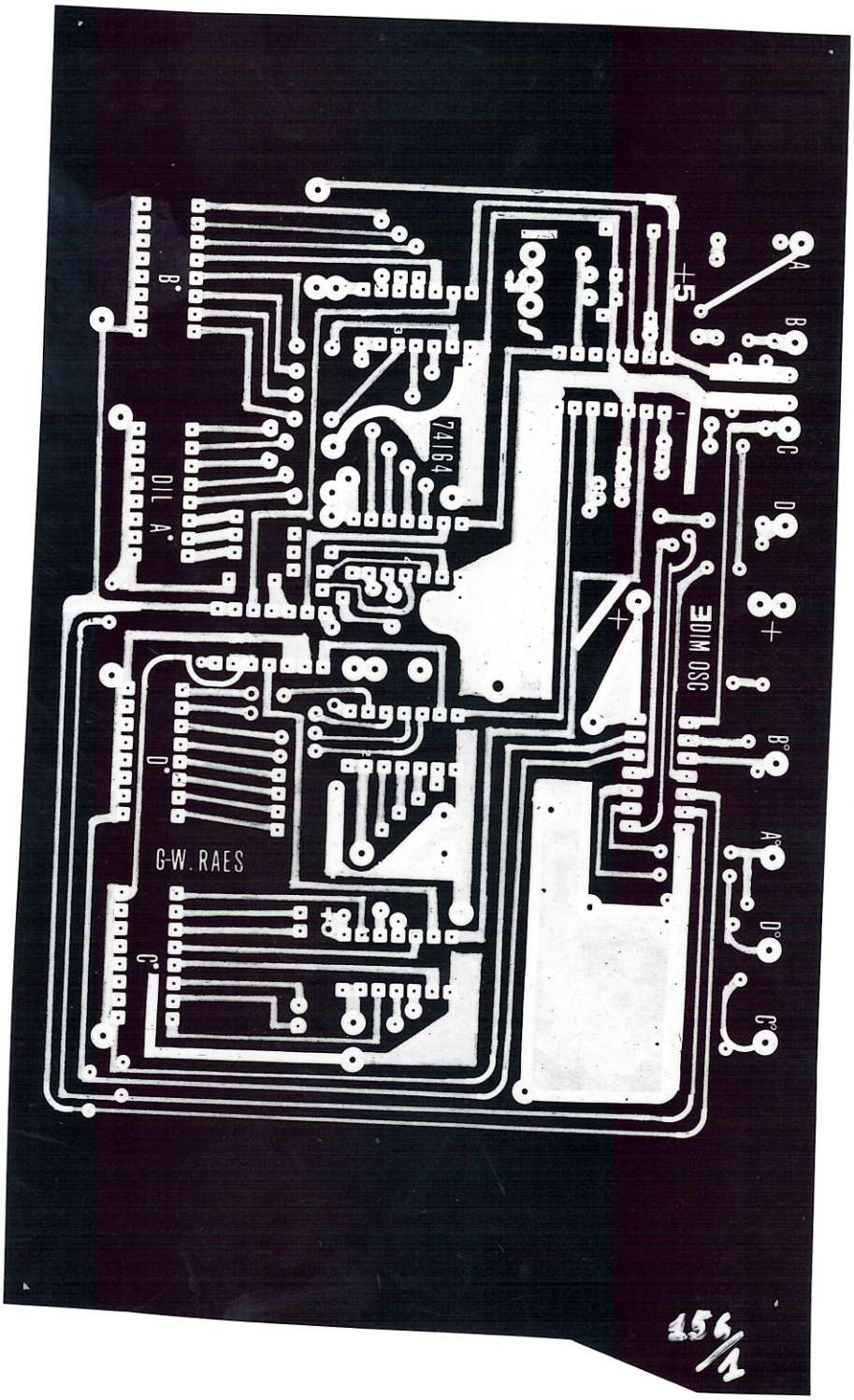



0
power drivers
+12 -18
N.C.
+15
0
-15
preamp power.
1
2
3
Ultrasound - receivers
1
2
3
4
driver outputs
1-2
3-4
JK
4°
3°
2°
1°
programm input
RCA
mod-n in/out
P3
1-2
3-4
OUT amps
modulo-n inputs
1
2
3
4
+12
+6
0
-6
-12
-18
-24
-30
-∞
12
6
0
6
12
18
24
30
∞
Q
ST
(8x1) into 4 Q osc.drivers
(2x4) + 4 into 2/4-ST/Q audio
logotronics 84
%
1
2
3
4
modulo-n dividers - programming switches





frekwentie karakteristiek driver trappen.


B°
DIL A°
74164
+5
A
B
C
D
OSC WIDE
B°
A°
D°
C°
D°
C°
C-W. RAES
151/1

Werkende koppels.

MC 2 [driver] → Hasberg 0,05 → piezo (OK)

TR 2 [receiver] → Hasberg 0,1 → Driver M5 (OK)

basgig, metalisch, geronmel.

(omkeerbaar systeem)

MC 1 [driver] → zachte veer, koop → piezo (OK)

Ø 7mm.

ca. 1 meter

Drone moniek

(met lage sinus

gestuurd)

Galm-veer set (ready-made) (OK)

→ als modulo-n systeem zeer goed + VS-driver input

Receivers

Piezo - Quad set

M1, M2 } originel Timeframes 2000 Ω

M3, M4 } reserve " 2000 Ω

→ Bim-box 40dB

GV1B Galm receivers Blauw

GV2B " Blauw

Drivers.

MC 1
MC 2 — uit oude kooptelefoon membraan gedempt met siliconen. Vijzaansluiting.

alleen bruikbaar als drivers.

LS 1
LS 2 } origineel timeframes 8Ω 0,1W 0,2W

LS 3
LS 4 } reserve "

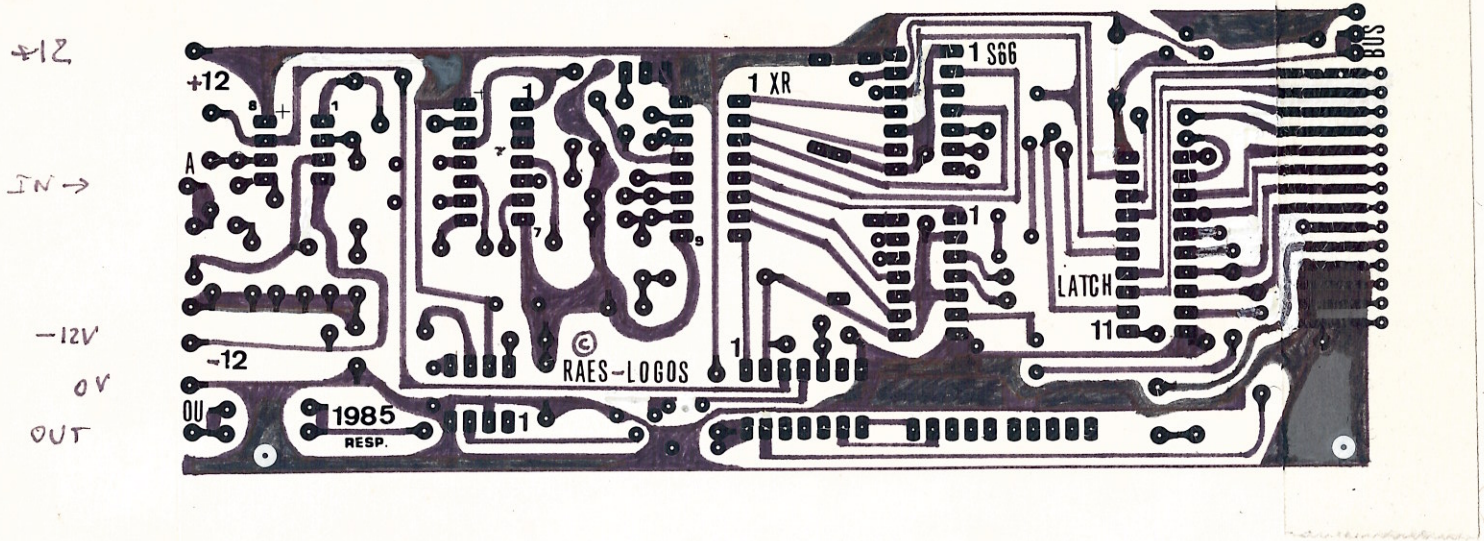
GV 1 Galmveerdrivers Rood (minijack)
GV 2 " " " Rood 16Ω 300mW – max.

M 5

TR 1
TR 2 } staallamel-transducers. omkeerbaar

3-dim. oscillator 1985/1.

TL082 40106 2240 4066 74LS373.



+12

IN →

−12V

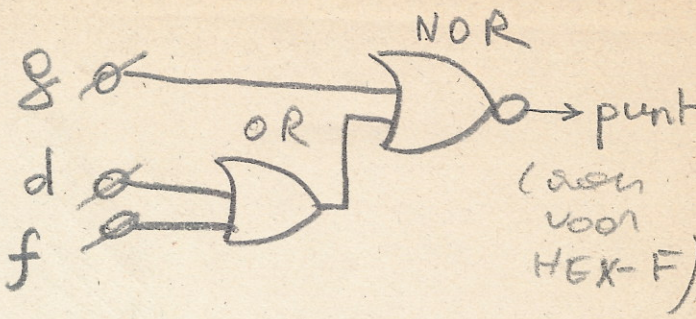
0V

OUT

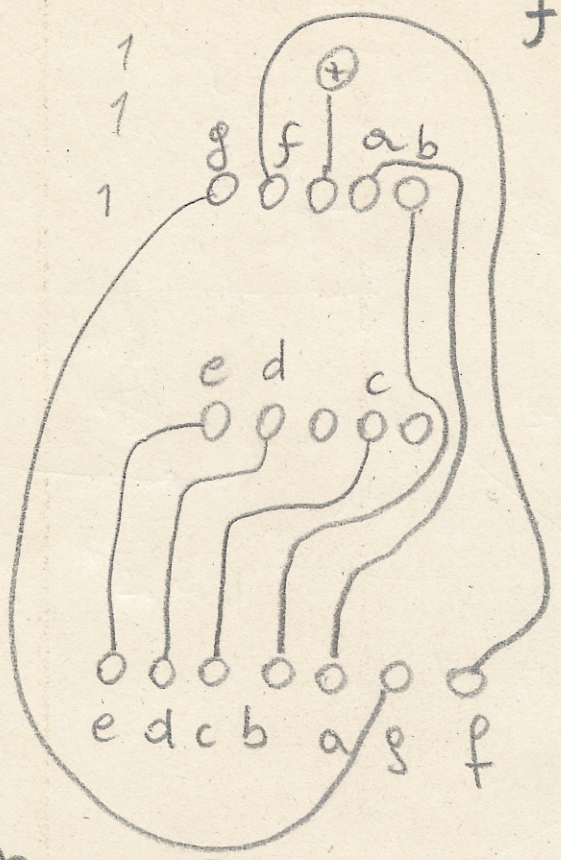
8 bit databus.
(3-state)

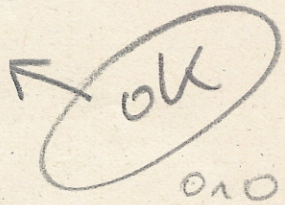
AND Nand

A	B		
1	1	1	0
0	1	0	1
1	0	0	1
0	0	0	1

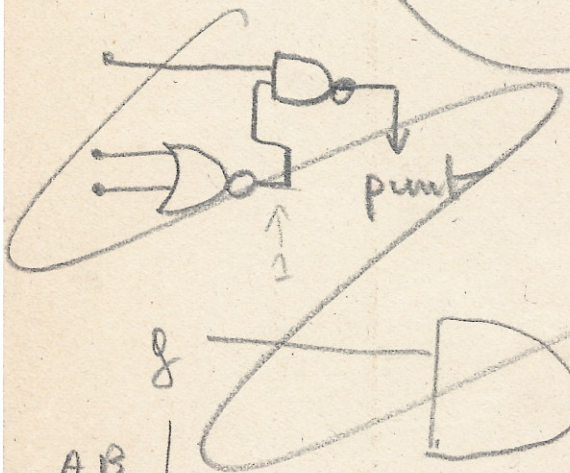


display kant.
(solderen aan koperzijde!

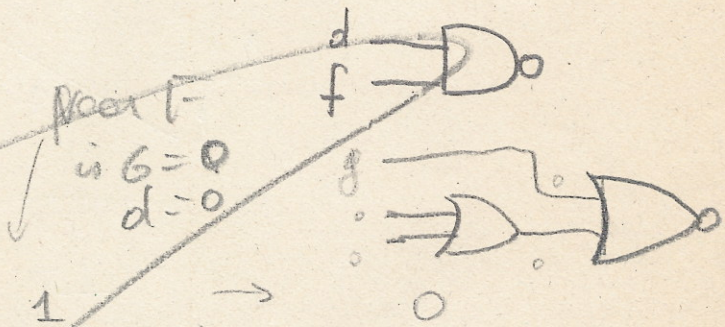


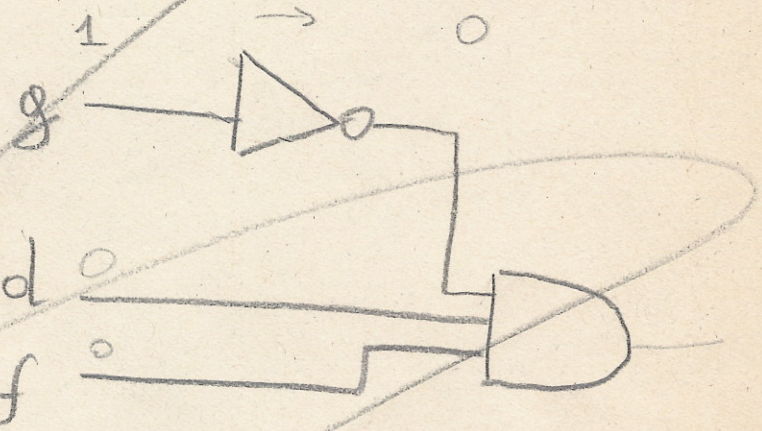


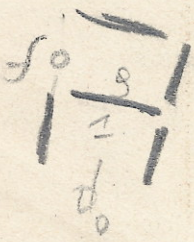
0 1 0 1 0 = 1

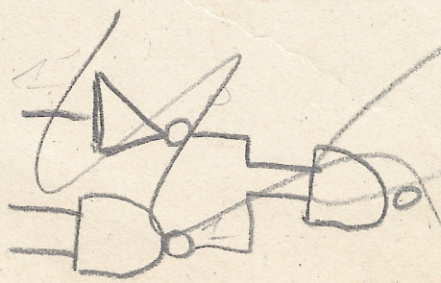


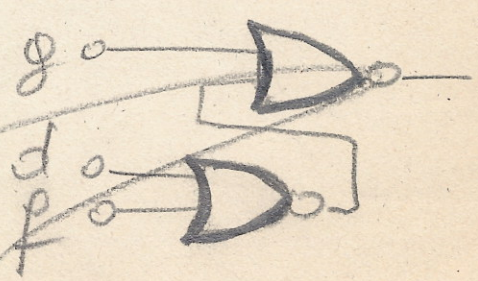
A B	
0 0	1
0 1	0
1 0	0
1 1	0

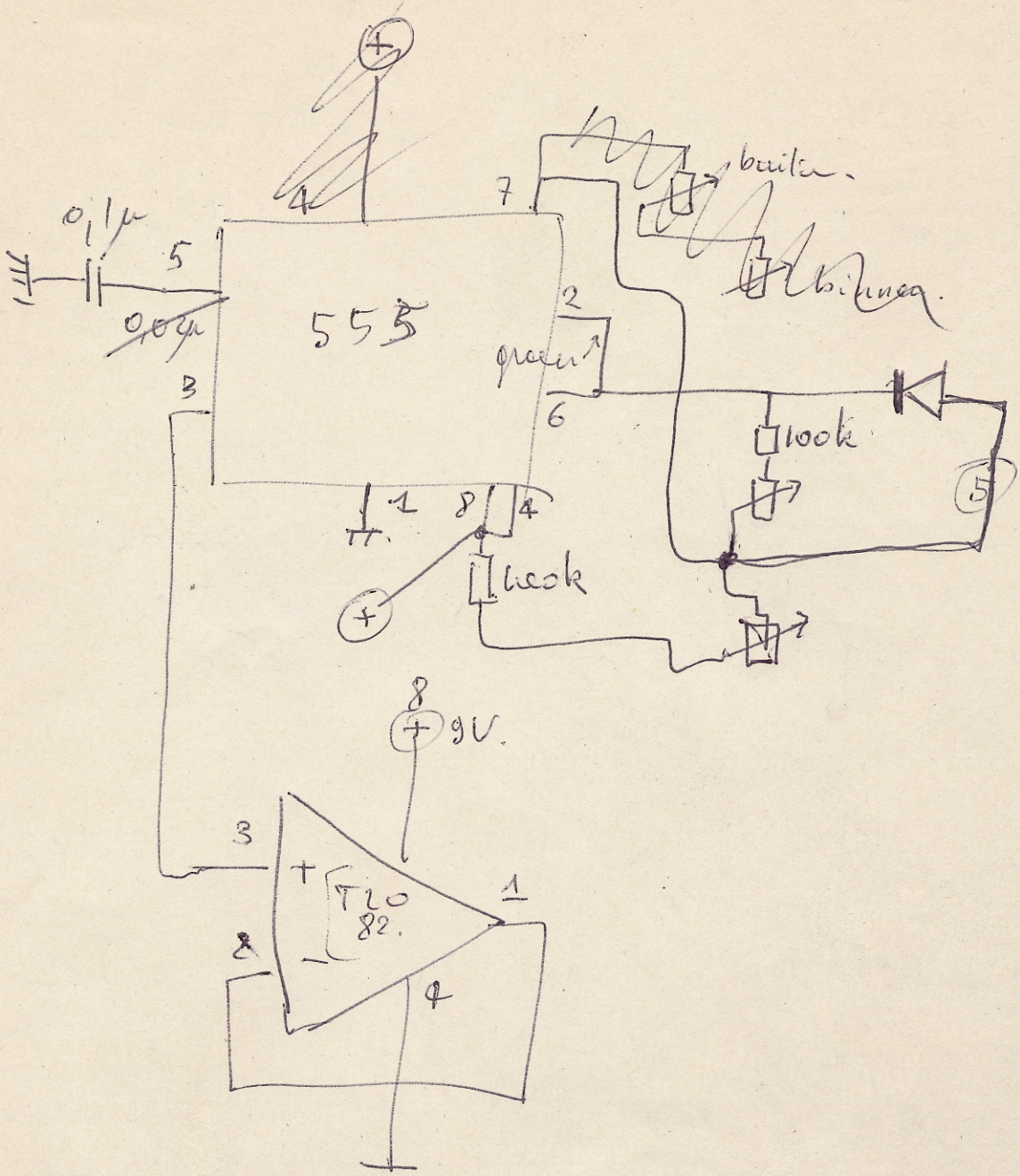




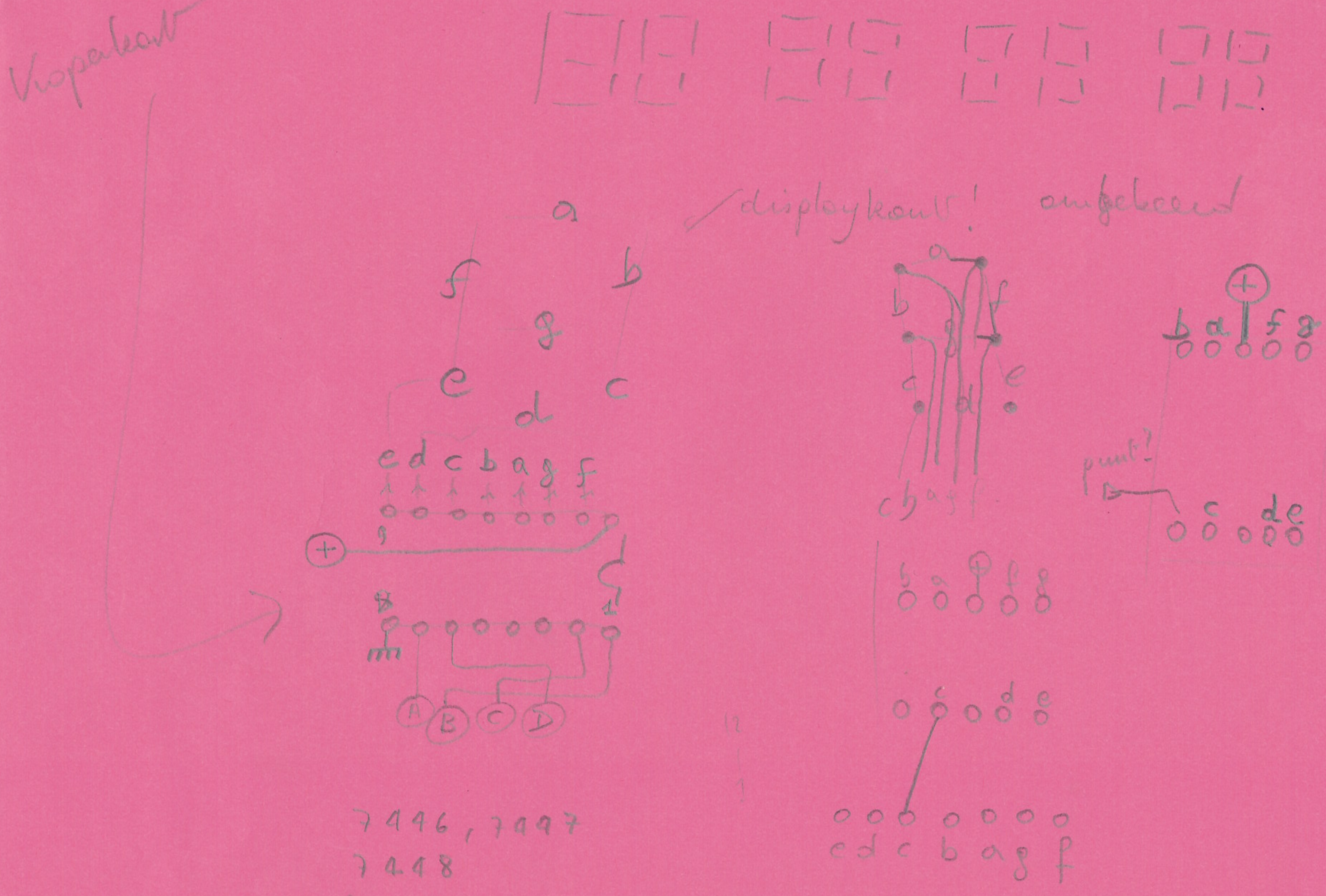








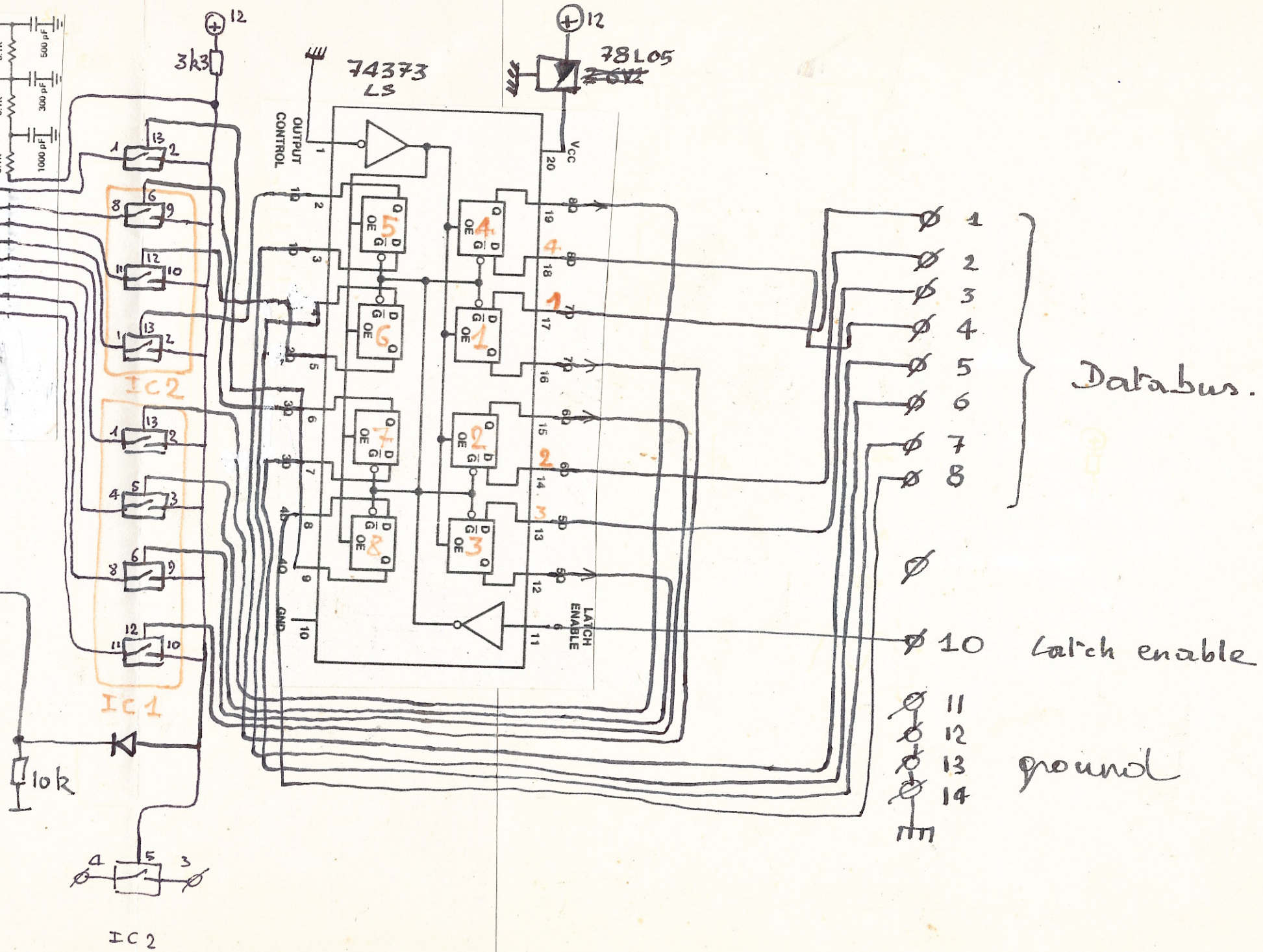
Y2.

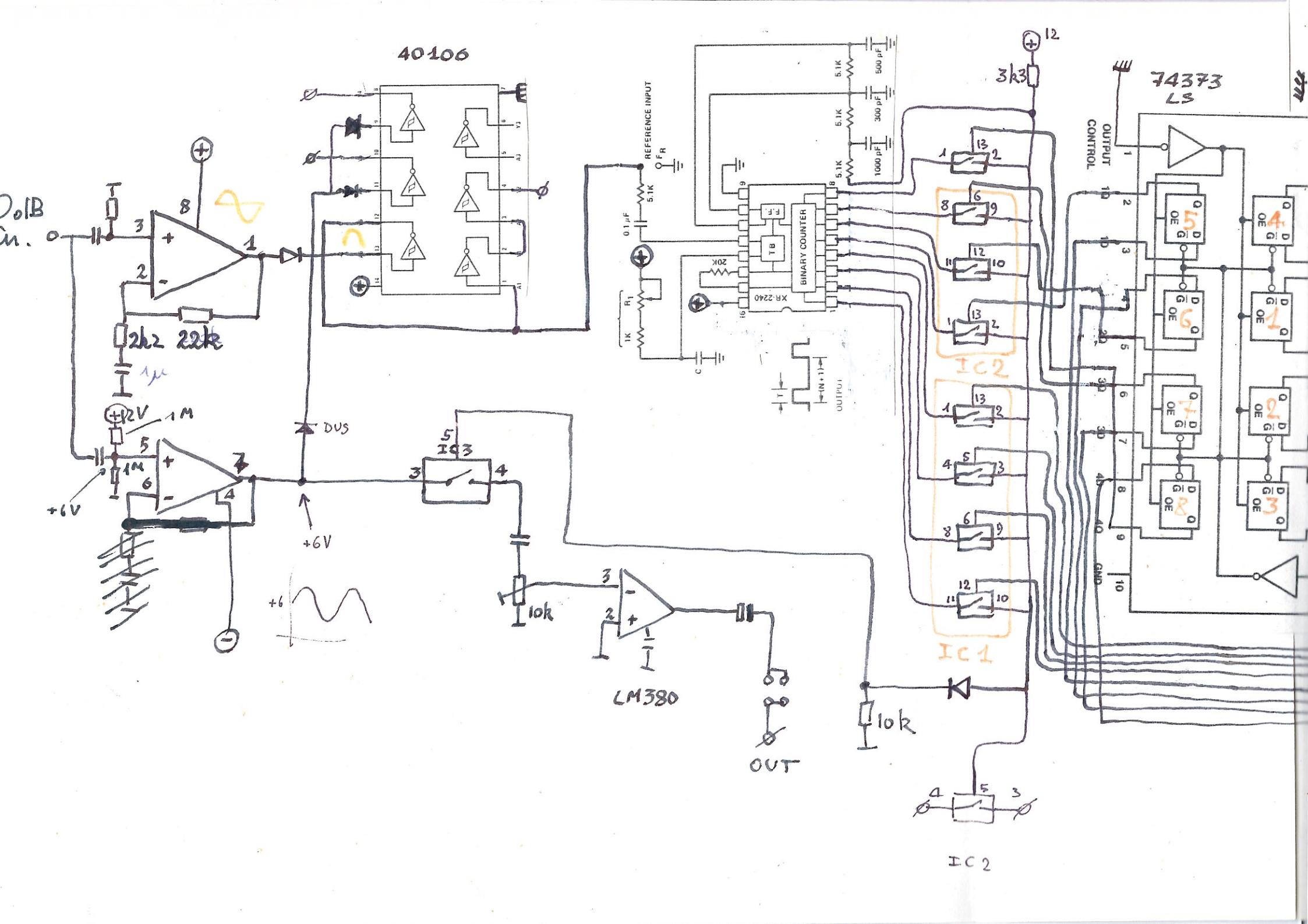


TIL 710
FND 507
TIL 321

7446, 7447
7448
of h-vlt-type
uitvoering

A = LSB   D = MSB


12
3k3
74373
LS
78L05
OUTPUT CONTROL
VCC
LATCH ENABLE
GND
IC2
IC1
10k
500 pF
300 pF
1000 pF
1
2
3
4
5
6
7
8
Databus.
10
Latch enable
11
12
13
14
ground
IC 2


40106
74373
LS
OUTPUT CONTROL
REFERENCE INPUT
BINARY COUNTER
XR-2240
3k3
2k2
22k
1µ
12V
1M
DUS
+6V
10k
LM380
OUT
IC2
IC1
IC3
GND

Mogelijke problemen Testfaze

* opgelet: Signaal in op ok
  ? 4066's
  moet rond $\frac{U_+}{2}$ lopen!

  ⇒ shift DC level up!

  (U_{ee} = ground)

* level aanpassingen lussen
  LATCH & 4066's

⇒ LATCH werkt op 0 + 5V voeding

LATCH U_{out} stuurt C-Mos Switches
met U_{out} = 4,5V minimaal

? Volstaat dit voor omschakeling?
4066.

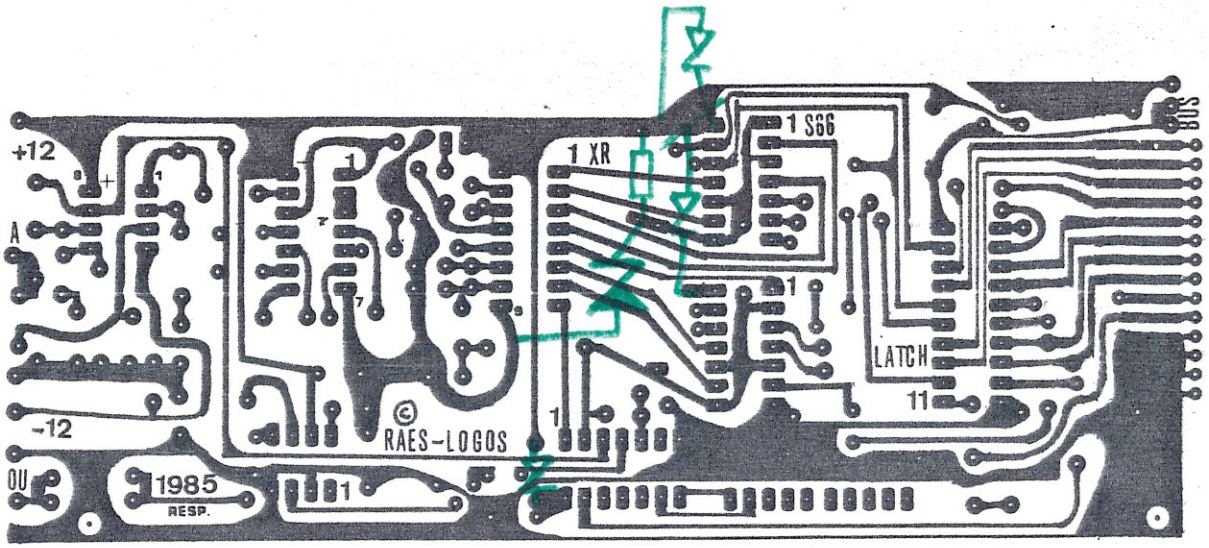
als 4066 gevoed wordt met 12 Volt

		9V	4,5V
moet	$U_1 \geq 8{,}4V$	6,3	3,15 V
	$U_0 \leq 2{,}4V$	1,8	0,9 V

⇒ 3k3 weerstand vervangen
& voedingsspanning 4066 verlagen!

TL082 40106

2240 4066 74LS373.



+12

IN →

−12V

0V

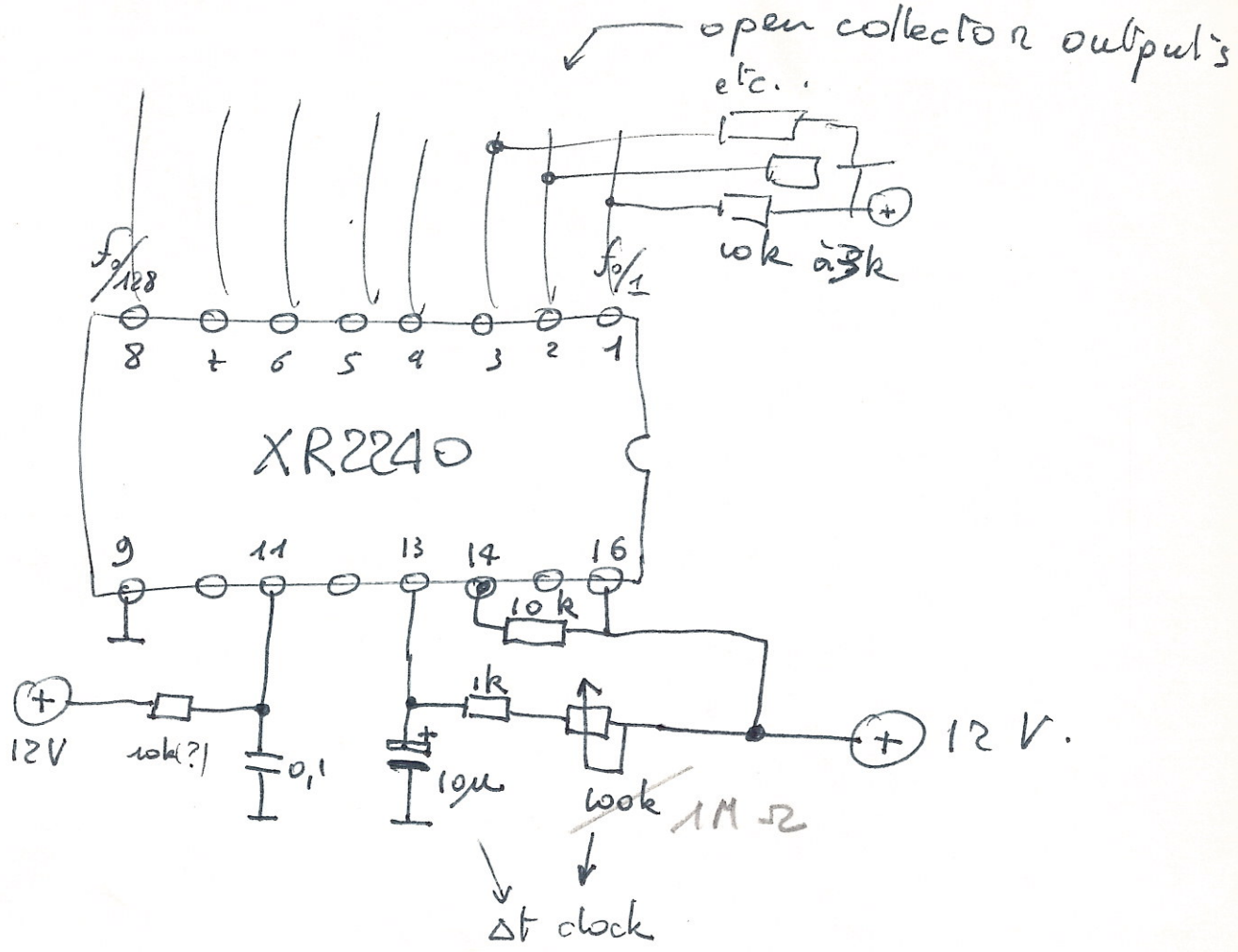
OUT

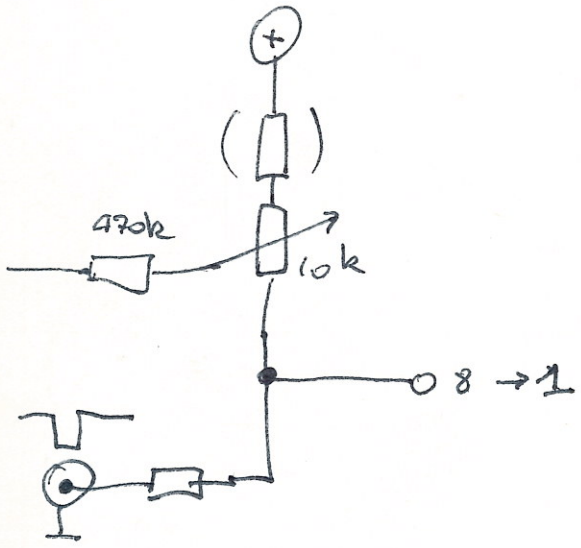
8 bit databus.
(3-state)

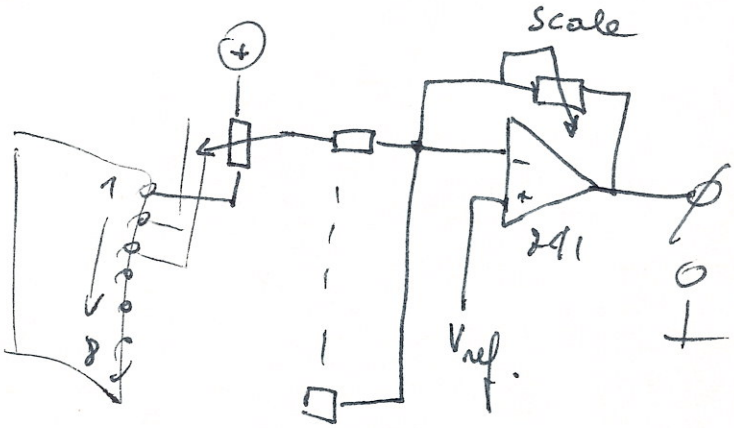
1) XR2240 heeft open collector-outputs
→ evt. met Zenerdioode
‖ U_{max} verlagen voor
aanpassing op C-mos schakelaars
(Z = 5V6 bvb.)

2) Voedingsspanning C-mos schakelaars (3x)
verlagen naar ca. 5V
met Zenerdiooles in serie met
de voedingsp +12 en pin 14.

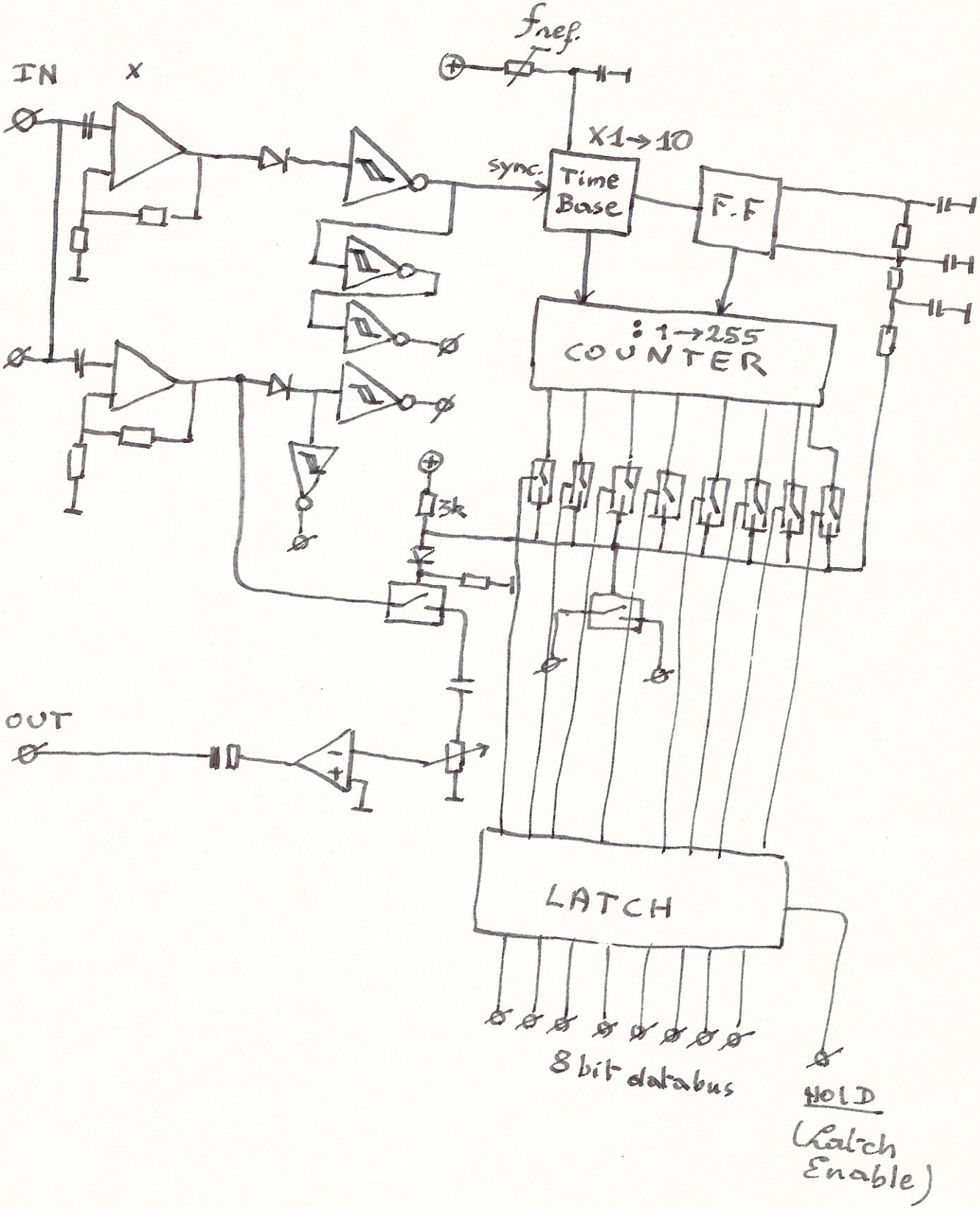
Adder - Counter - Sequencer - Timer.





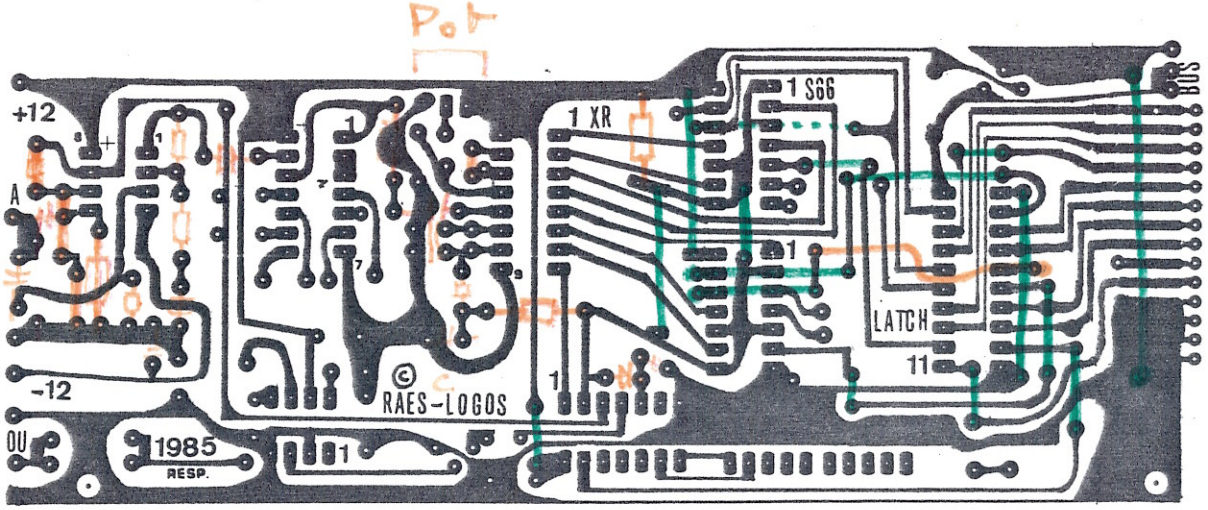


Principe - schema.



TL082 40106 2240 4066 74LS373.

Bestukkings plan & schaduppen.

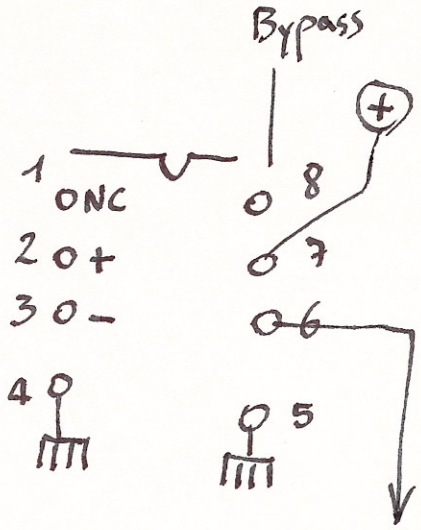


LM380 8p.

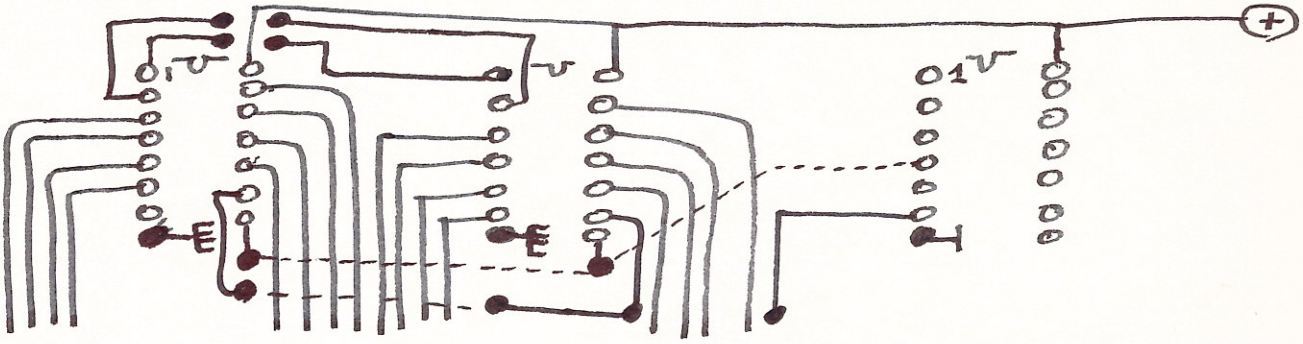
8 bit databus. (3-staten)

→ in produktie (1 exp!)

Vn. 3-dimensionele oscillatoren.


Bypass
+
1
NC
8
2
+
7
3
-
6
4
5

40106
of
7414



4558 +voetje

14p-voetje m. 40106

3 voetjes 4066

5k1 IIII

0,1µ

DUS

1k II

Zener 5V6

20k

1nF

300pF

500pF

LM 380 8pin.

10k

DUS

3k

7414 HC.

→ $U_{supp.} \leq \underline{\underline{7V}}$!

MC14558 BCP

XR2240 : 4 – 15V

4066 : 0 – 15V (12)

±12V 24V$_{pp}$

→ 20V$_{pp}$ bereik

$\frac{10V}{\sqrt{2}} = 7V.$

0,7 V in → 7 V$_{outr.}$ $A_V = 10$

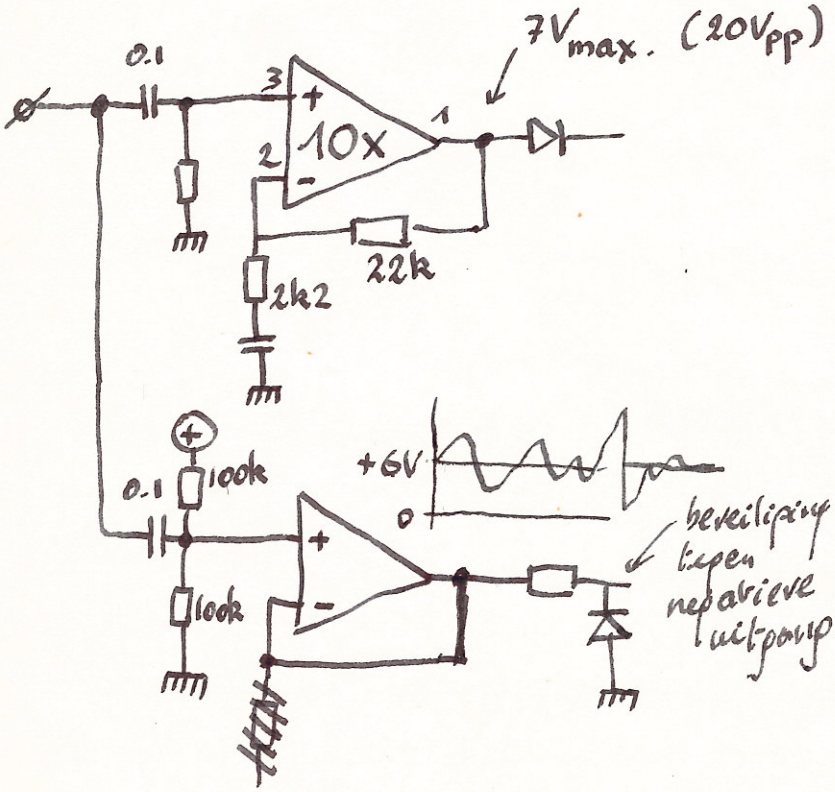
70 mV in → " $A_V = 100$

40 dB

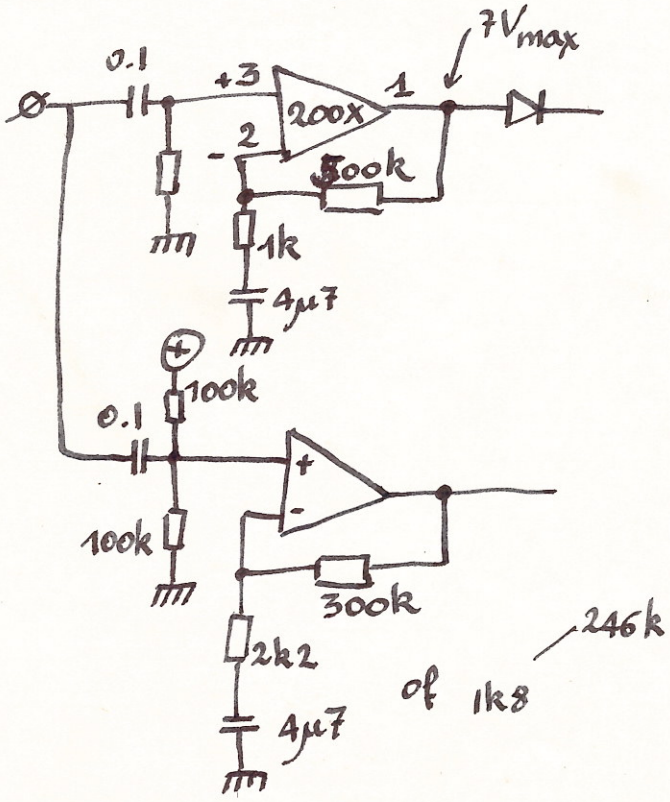
(M~~7~~8L XX AC 2.

Ingaapstrap:

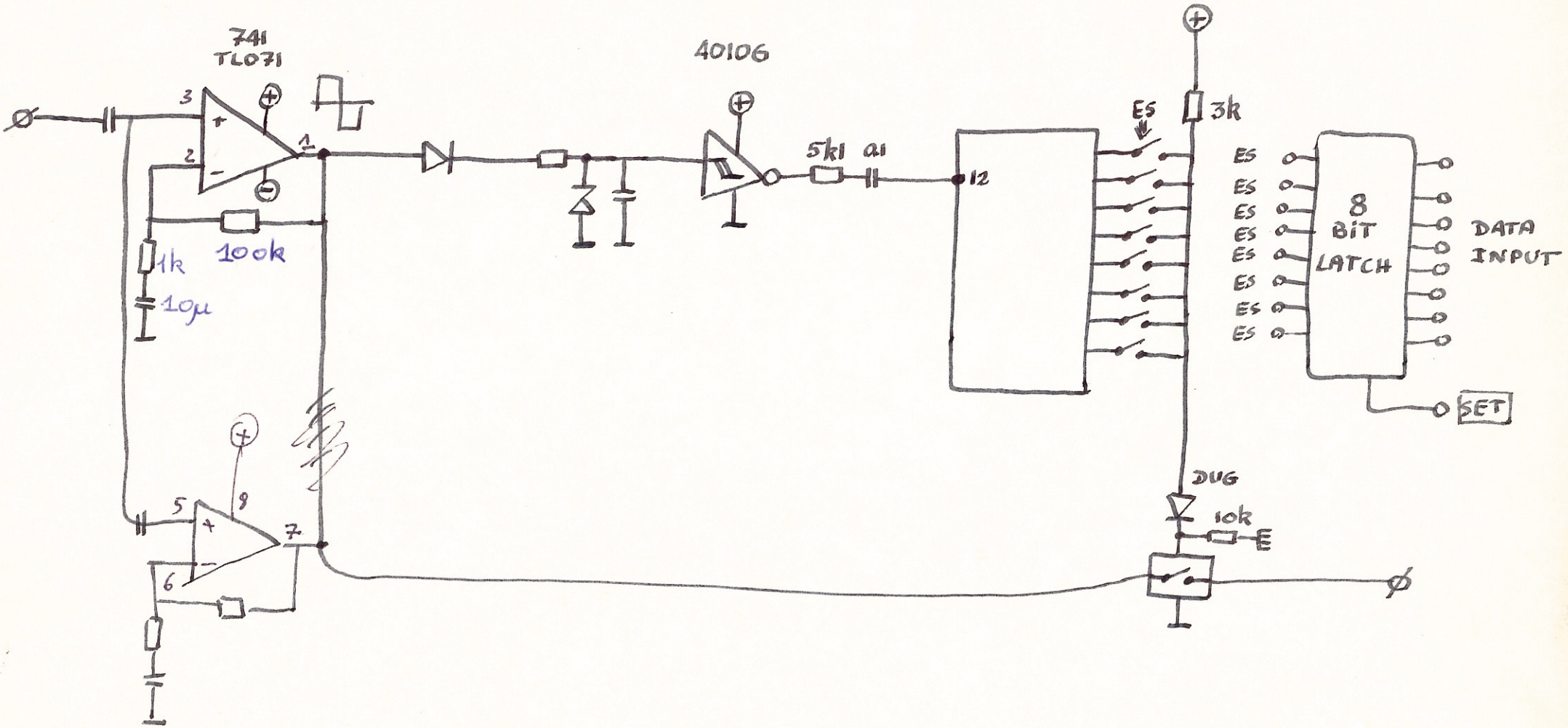
1. Voor U_{in} = 0dB



2. Voor U_{in} = -34dB (15,5 mVolt)

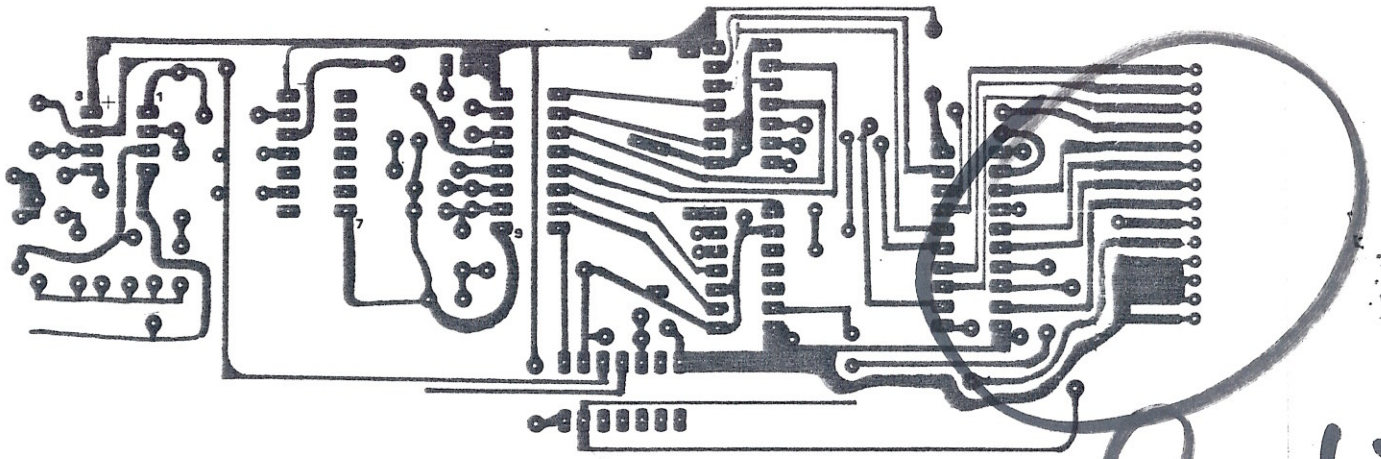


246k of 1k8


741
TL071
40106
3
2
1
1k
100k
10µ
5k1
a1
12
ES
3k
8
BIT
LATCH
DATA
INPUT
SET
DUG
10k
E
5
9
7
6

TL082 40106

2240 4066 74LS373.



Paul-

BINARY PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the XR-2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 5 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

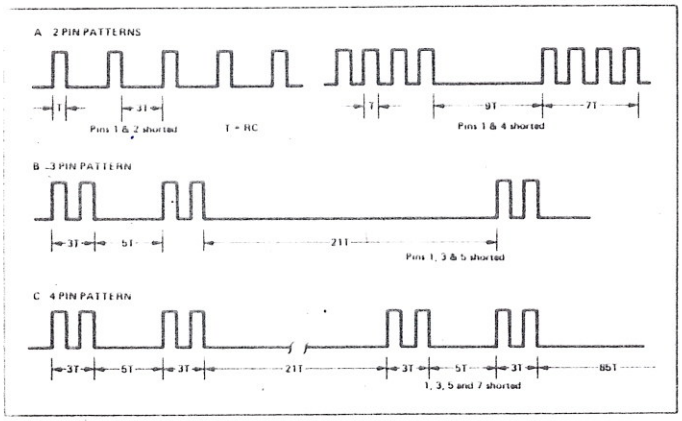


Figure 22. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

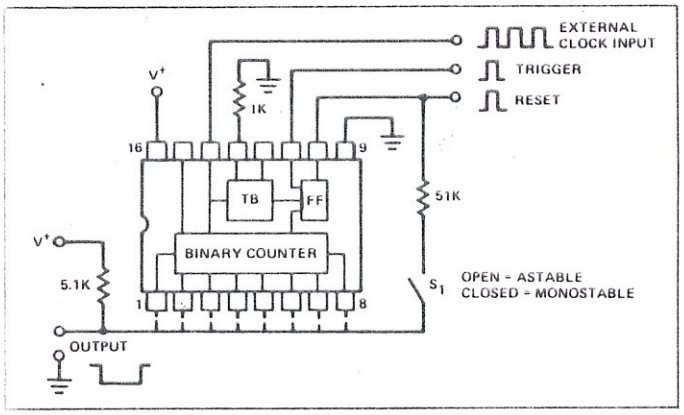


Figure 23. Operation with External Clock

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be $\geq 1\ \mu S$.

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V^+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of XR-2240 can be used to generate 255 discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N+1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 4 are connected together to the output bus, the total count is: N=1+4+8=13; and the period of the output waveform is equal to (N+1) T or 14T. In this manner, 256 different frequencies can be synthesized from a given time-base setting.

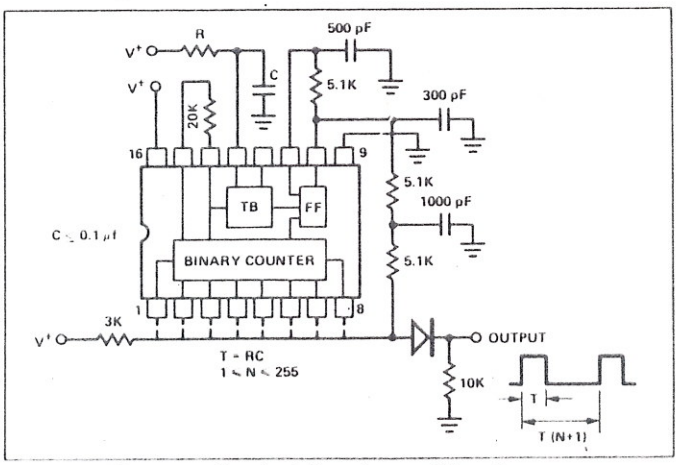


Figure 24. Frequency Synthesis from Internal Time-Base

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 16 and 17 for external sync waveform and harmonic capture range.) If the the time base is synchronized to $(m)^{th}$ harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 25 can produce 1500 separate frequencies from a single fixed reference.

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

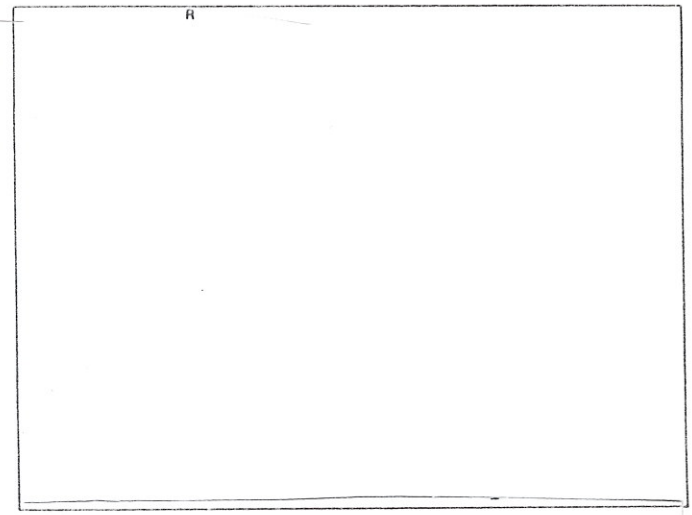


Figure 25. Frequency Synthesis by Harmonic Locking to an External Reference

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics

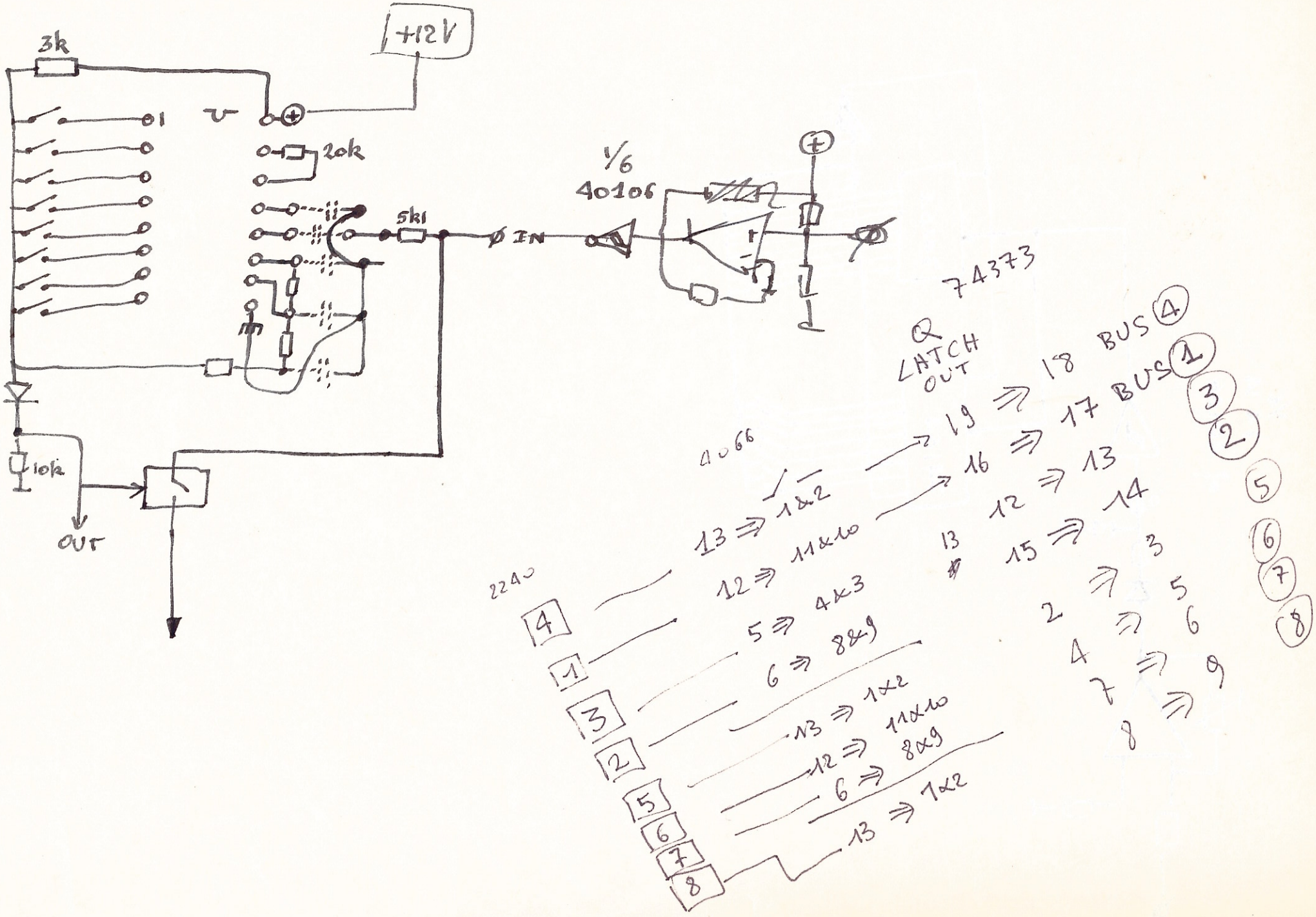
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_I	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, OC = V_{IH} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.


3k
+12V
20k
5k1
Ø IN
1/6
40106
10k
OUT
74373
Q
LATCH
OUT
4066
13 ⇒ 1x2
12 ⇒ 11x10
5 ⇒ 4x3
6 ⇒ 8x9
19 ⇒ 18 BUS 4
16 ⇒ 17 BUS 1
12 ⇒ 13
15 ⇒ 14
2240
4
1
3
2
5
6
7
8
13 ⇒ 1x2
12 ⇒ 11x10
6 ⇒ 8x9
13 ⇒ 1x2
2 ⇒ 5
4 ⇒ 6
7 ⇒ 9
8 ⇒ 3

National Semiconductor

microCMOS

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

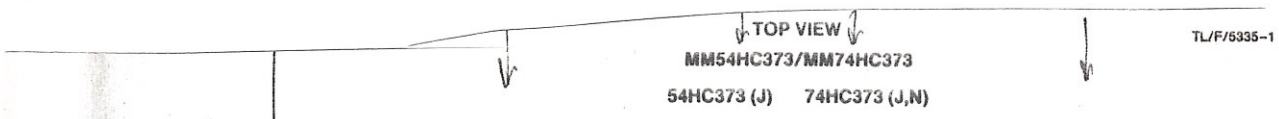
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5335–1

MM54HC373/MM74HC373

54HC373 (J) 74HC373 (J,N)

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	H
L	L	X	Q_0
H	X	X	Z

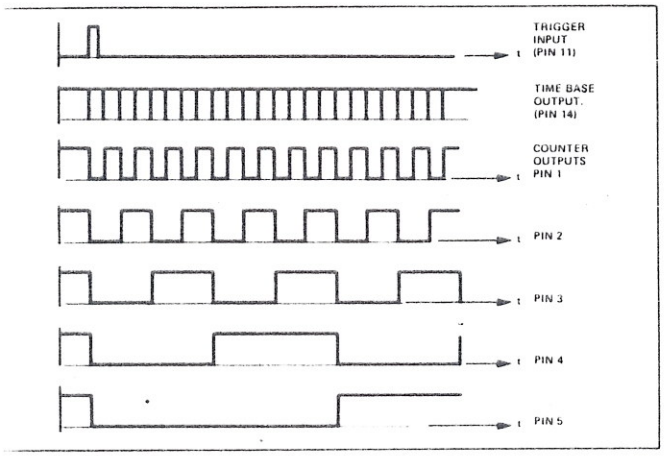
H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

RINCIPLE OF OPERATION

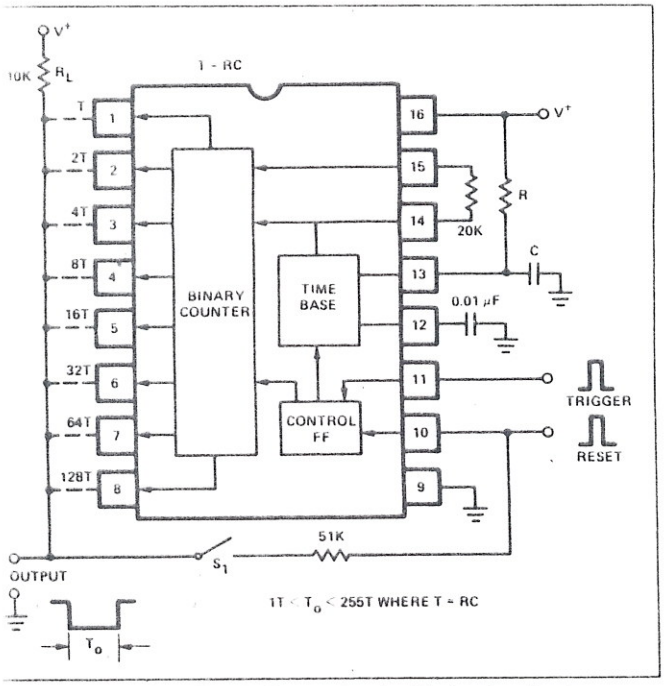
ie timing cycle for the XR-2240 is initiated by applying a sitive-going trigger pulse to pin 11. The trigger input actu- es the time-base oscillator, enables the counter section, and ts all the counter outputs to "low" state. The time-base cillator generates timing pulses with its period, T, equal to RC. These clock pulses are counted by the binary counter ction. The timing cycle is completed when a positive-going set pulse is applied to pin 10.



gure 5. Timing Diagram of Output Waveforms

gure 5 gives the timing sequence of output waveforms at rious circuit terminals, subsequent to a trigger input. When e circuit is at reset state, both the time-base and the counter tions are disabled and all the counter outputs are at "high" ate.

most timing applications, one or more of the counter out- its are connected back to the reset terminal, as shown in gure 6, with S_1 closed. In this manner, the circuit will start ning when a trigger is applied and will automatically reset elf to complete the timing cycle when a programmed count completed. If none of the counter outputs are connected k to the reset terminal (switch S_1 open), the circuit would erate in its astable or free-running mode, subsequent to a gger input.



gure 6. Generalized Circuit Connection for Timing Applications witch S_1 Open for Astable Operations, Closed for Monostable perations)

PROGRAMMING CAPABILITY

The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 6. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$, where $T = RC$.

TRIGGER AND RESET CONDITIONS

When power is applied to the XR-2240 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 5.

The counter outputs can be used individually, or can be connected together in a "wired-or" configuration, as described in the Programming section.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs are shown in Figure 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 13). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 16. Recommended sync pulse widths and amplitudes are also given in the figure.

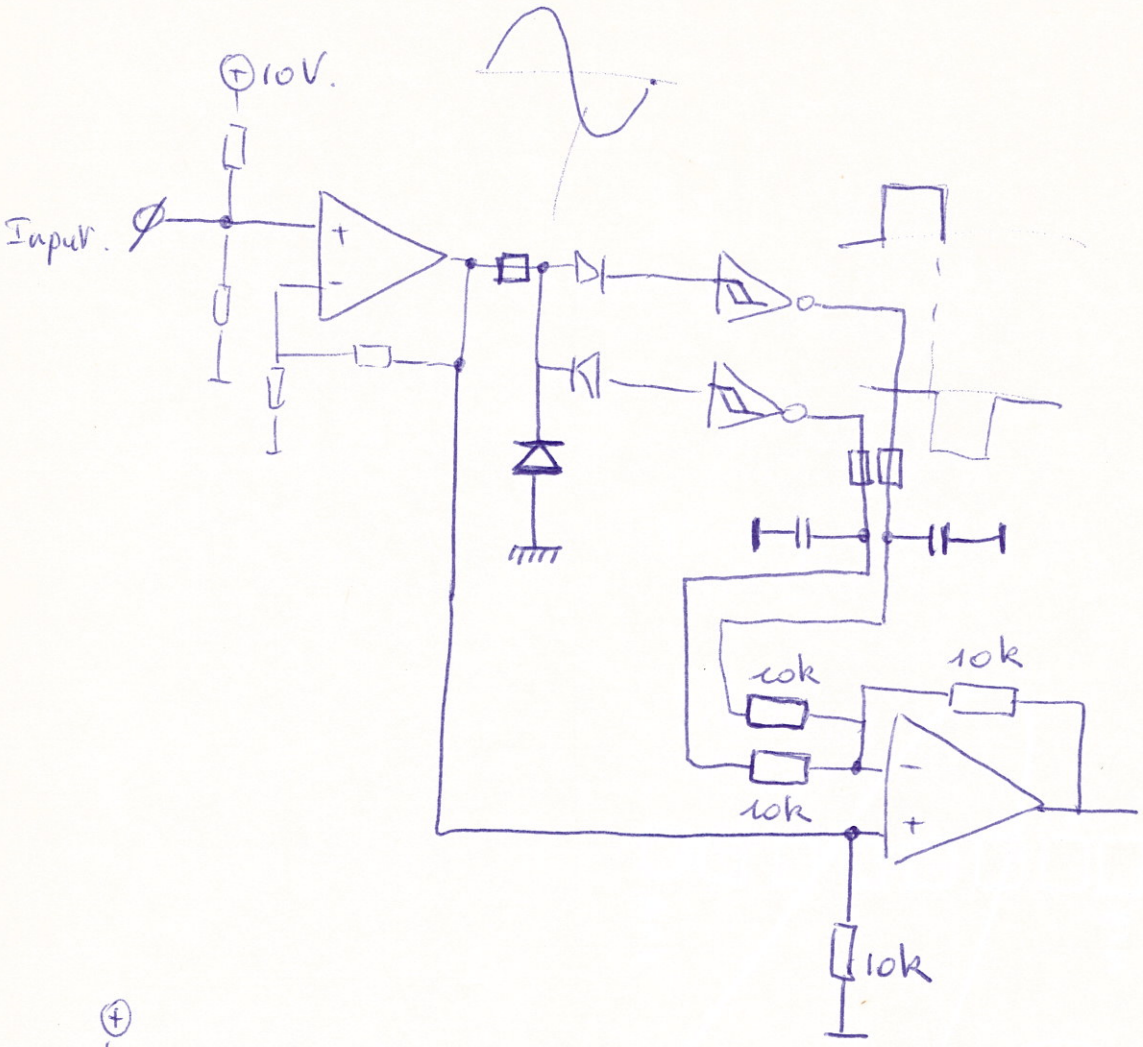
HARMONIC SYNCHRONIZATION

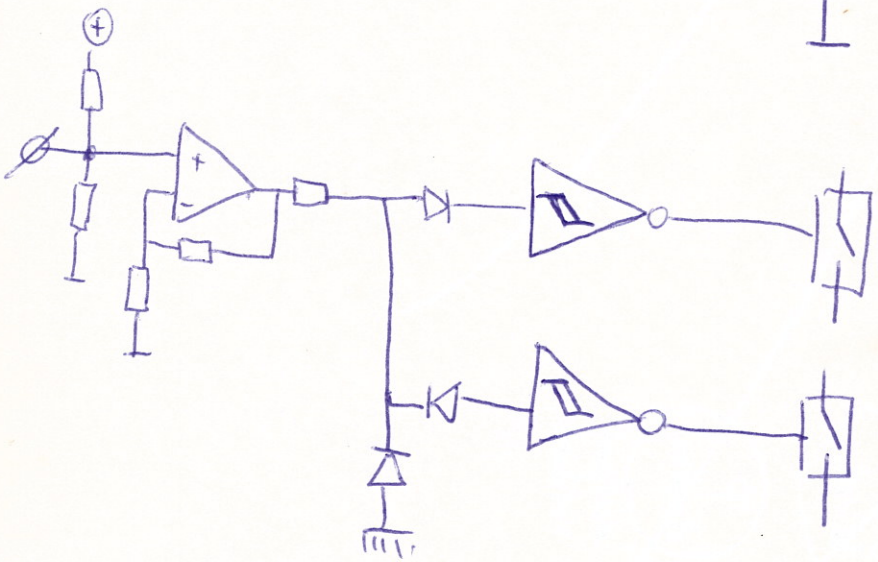
Time-base can be synchronized with *integer multiples or harmonics* of input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$

$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 17 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.


+10V.
Input.
10k
10k
10k
10k



Circuit Operation:

With reference to Figure 1, the operation of the synthesizer circuit can be briefly explained as follows: The reference input frequency, f_R, is applied to the time-base sync terminal (pin 12) through a 5.1 KΩ series resistance and a coupling capacitor. The recommended waveform for the input frequency, f_R, is a 3 Vpp pulse train with a pulse width in the range of 30% to 80% of the time-base period, T. The multiplication factor M is chosen by the potentiometer R_1 which sets the time-base period T (T = RC). If no external reference is used, then M is automatically equal to 1.

The divider modulus, N, is chosen by shorting various counter outputs to a 3K common pull-up resistor. The output waveform is a pulse train with a fixed pulse width, T = RC, and a period $T_O = (N + 1)RC$.

The external R-C network between the output and the trigger and reset terminals of the XR-2240 is a non-critical delay network which resets and re-triggers the circuit to maintain a periodic output waveform. For the component values shown in Figure 1, the circuit can operate with the timing components R and C in the range of:

$$0.005\ \mu F \leq C \leq .1\ \mu F;\ 1\ K\Omega \leq R \leq 1\ M\Omega$$

The XR-2240 is a low-frequency circuit. Therefore, the maximum output frequency is limited to ≈200 kHz, by the frequency capability of the internal time base oscillator.

A particularly useful application of the simple synthesizer circuit of Figure 1 is to generate stable clock frequencies which are synchronized to an external reference, such as the 60 Hz line frequency. For example, one can generate a 100 Hz reference synchronized to 60 Hz line frequency simply by setting M = 5 and N = 2 such that:

$$f_O = f_R \frac{M}{1+N} = (60)\frac{5}{1+2} = 100\ Hz$$

C = 10nF

R = 470k ---- 1k

$RC = 4{,}7 \cdot 10^{-3}$ 10^{-5}

$\frac{1}{RC} = 212\ Hz.$ 100kHz.

beter: kies C = 33nF

R = 470k pot. .... 1k min.

RC = 0,0155 s tot $3{,}3.10^{-5}$

f_0 $\frac{1}{RC} = 64\ Hz$ tot 30kHz.

Application Note AN-07

Single-Chip Frequency Synthesizer Employing the XR-2240

INTRODUCTION

The XR-2240 monolithic timer/counter contains an 8-bit programmable binary counter and a stable time-base oscillator in a single 16-pin IC package. Although the circuit was originally designed as a long-delay timer capable of generating time delays from microseconds to weeks, it also offers a wide range of other applications beyond simple time-delay generation. One such unique application is its use as a single-chip, frequency synthesizer, where it can generate over 2,500 discrete frequencies from a single reference frequency input.

The operation of the XR-2240 as a frequency synthesizer is possible because of the ability of the circuit to both *multiply* and *divide* the input frequency reference. It can, simultaneously, multiply the input frequency by a factor, "M," and divide it by a factor "N + 1," where both M and N are adjustable integer values. Therefore, the circuit can produce an output frequency, f_O, related to the input reference frequency f_R as:

$$f_O = f_R \frac{M}{1+N}$$

Figure 1 shows the circuit connection for operating the XR-2240 timer/counter as a self-contained frequency synthesizer. The integer values M and N can be externally adjusted over a broad range:

$$1 \leqslant M \leqslant 10 \quad 1 \leqslant N \leqslant 255$$

The multiplication factor M is obtained by locking on the harmonics of the input frequency. The division factor N is determined by the pre-programmed count in the binary counter section. The principle of operation of the circuit can be best understood by briefly examining its capabilities for frequency division and multiplication separately.

Frequency Division by (1 + N):

When there is no external reference input, f_R, the time-base oscillator section of the XR-2240 free-runs at its set frequency, f_S ($f_S = 1/RC$), where R and C are the external components at pin 13. The 8-bit binary counter can be programmed to divide the time-base frequency by an integer count, N, and generate an output pulse train whose frequency is:

$$f_O = f_S \frac{1}{1+N}$$

Frequency Multiplication by "M":

Frequency multiplication is achieved by synchronizing the time-base oscillator with the *harmonics* of the input sync or reference signal. Thus, if the time-base oscillator is made to free-run at "M" times the input frequency, it can be made to synchronize with the "M"th harmonic of the input reference signal. Typical capture range of the circuit is better than ±3%, for values of $1 \leqslant M \leqslant 10$; and since the time-base is accurate to within ±0.5% of the external R-C setting, lock-up does not present a problem for a given harmonic lock setting.

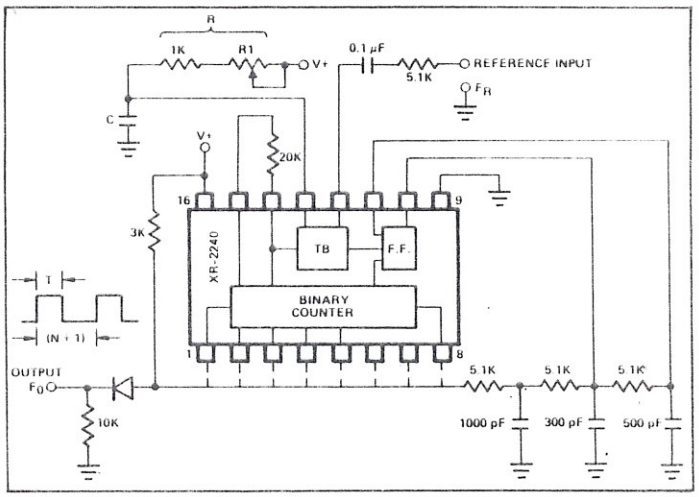


Figure 1.

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.

CHARACTERISTICS	XR-082M/XR-083M			XR-082/XR-083			XR-082C/XR-083C XR-082D/XR-083D			UNITS	SYMBOL	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Input Offset Voltage		3	6 9		3	6 9		5	15 20	mV mV	V_{OS} V_{OS}	$R_S = 50\Omega$, $T_A = 25°C$ $R_S = 50\Omega$, T_A = Full Range
Offset Voltage Temp. Coef.		10			10			10		$\mu V/°C$	$\Delta V_{OS}/\Delta T$	$R_S = 50\Omega$, T_A = Full Range
Input Bias Current XR-082C/XR-083C XR-082D/XR-083D		30	200		30	200		 30 100	 400 800	 pA pA pA	I_B	$T_A = 25°C$, Note 3
Input Bias Current Over Temp.			50			20			20	nA	I_B	T_A = Full Range
Input Offset Current XR-082C/XR-083C XR-082D/XR-083D		5	100		5	100		 5 20	 200 400	 pA pA pA	I_{OS}	$T_A = 25°C$, Note 3
Input Offset Current Over Temp.			20			10			5	nA		T_A = Full Range
Supply Current (per amplifier)		1.4	2.8		1.4	2.8		1.4	2.8	mA	I_{CC}	No Load, No Input Signal
Input Common Mode Range	±12			±12			±10			V	V_{iCM}	
Voltage Gain	 50 25	200		 50 25	200		 25 15	200		V/mV	A_{VOL}	$R_L \geq 2$ KΩ, $V_O = \pm 10V$ $T_A = 25°C$ T_A = Full Range
Max. Output Swing (peak-to-peak)	 24 24	27		 24 24	27		 24 24	27		V	V_{OPP}	$R_L \geq 10$ KΩ $T_A = 25°C$ T_A = Full Range
Input Resistance		10^{12}			10^{12}			10^{12}		Ω	R_{in}	$T_A = 25°C$
Unity-Gain Bandwidth		3			3			3		MHz	BW	$T_A = 25°C$
Common-Mode Rejection	80	86		80	86		70	76		dB	CMRR	$R_S \leq 10$ KΩ
Supply-Voltage Rejection	80	86		80	86		70	76		dB	PSRR	
Channel Separation		120			120			120		dB		$A_V = 100$, Freq. = 1 kHz
Slew Rate		13			13			13		V/μS	dV_{out}/dt	$A_V = 1$, $R_L = 2$ KΩ $C_L = 100$ pF, $V_I = 10V$
Rise Time Overshoot		0.1 10			0.1 10			0.1 10		μsec %	t_r t_o	$A_V = 1$, $R_L = 2$ KΩ $C_L = 100$ pF, $V_I = 20$ mV
Equivalent Input Noise Voltage		20			20			20		$nV/\sqrt{Hz}$	e_n	$R_S = 100\Omega$ f = 1 kHz

Note 1: For Supply Voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Note 3: XR-082C/XR-083C and XR-082D/XR-083D differ only in their Input Bias Current and Input Offset Current specifications.

XR-082/083

Dual BIFET Operational Amplifiers

GENERAL DESCRIPTION – ADVANCE INFORMATION

The XR-082/XR-083 family of junction FET input dual operational amplifiers are designed to offer higher performance than conventional bipolar op-amps. Each amplifier features high slew-rate, low input bias and offset currents, and low offset voltage drift with temperature. These operational amplifier circuits are fabricated using ion-implantation technology which combines well-matched junction FETs and high-performance bipolar transistors on the same monolithic chip.

The XR-082 family of dual BIFET op-amps are packaged in 8-pin dual-in-line packages. The XR-083 family of op-amps offer independent offset adjustment for each of the individual op-amps on the same chip, and are available in 14-pin dual-in-line packages.

FEATURES

Direct Replacement for TL082/TL083 (See Chart)
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short-Circuit Protection
High Input Impedance . . . FET Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew-Rate . . . 13 V/μs, Typical

Exar Part Number	Texas Instruments Equivalent
XR-082M/XR-083M	TL-082M/TL-083M
XR-082/XR-083	TL-082AI/TL-083AI
XR-082C/XR-083C	TL-082C/TL-083C
XR-082D/DX-083D	———

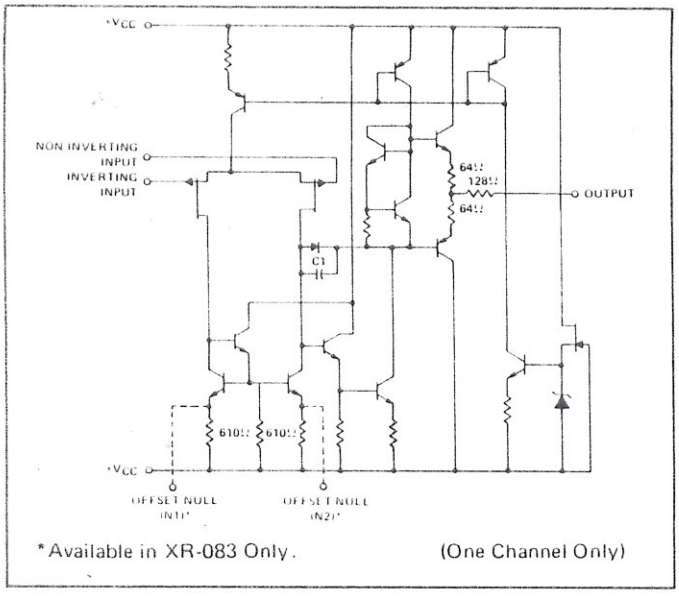
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short-Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW °C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	–65°C to +150°C

AVAILABLE TYPES

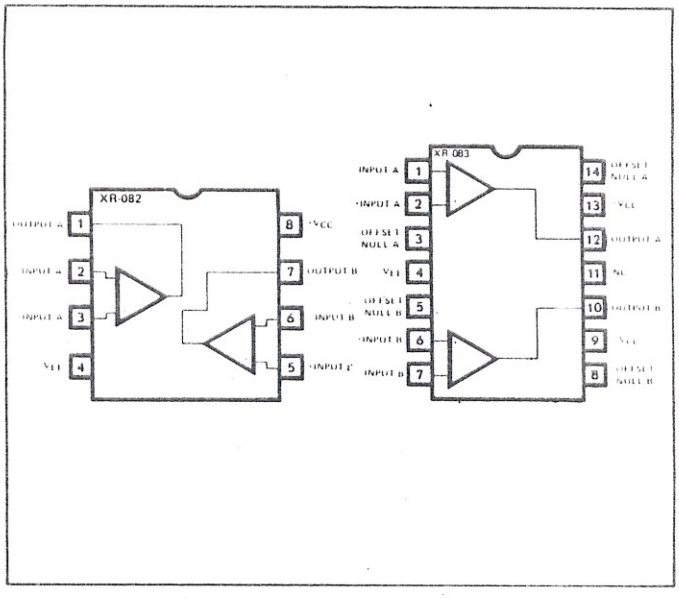
Part Number	Package	Operating Temperature
XR-082M/XR-083M	Ceramic	–55°C to +125°C
XR-082N/XR-083N	Ceramic	–25°C to +85°C
XR-082P/XR-083P	Plastic	–25°C to +85°C
XR-082CN/XR-083CN	Ceramic	0°C to +75°C
XR-082CP/XR-083CP	Plastic	0°C to +75°C
XR-082DN/XR-083DN	Ceramic	0°C to +75°C
XR-082DP/XR-083DP	Plastic	0°C to +75°C

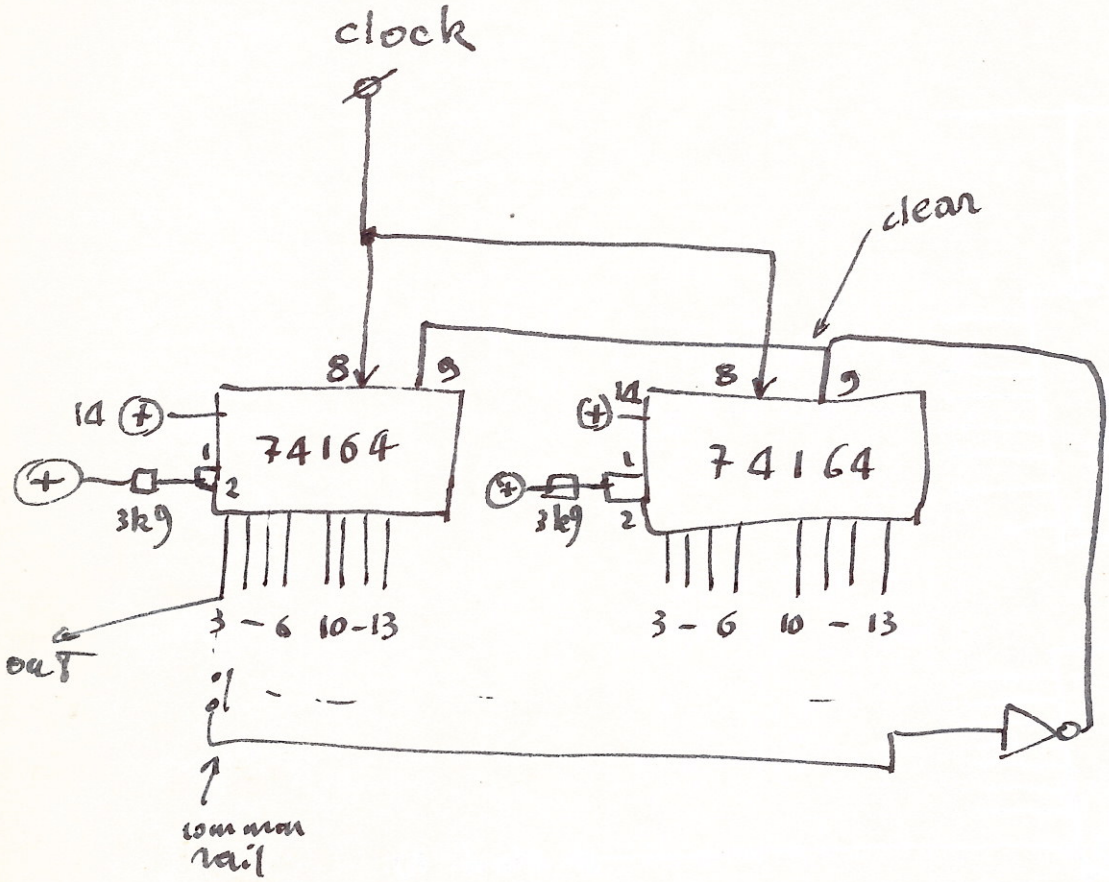
EQUIVALENT SCHEMATIC

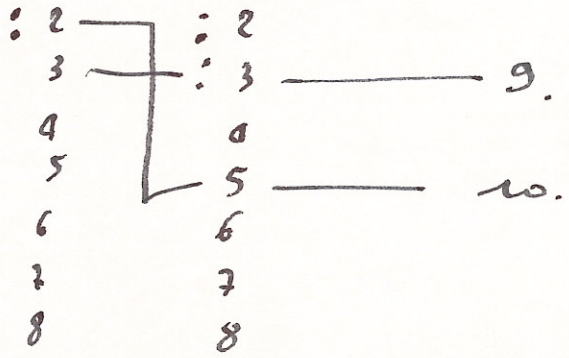


*Available in XR-083 Only. (One Channel Only)

FUNCTIONAL BLOCK DIAGRAM




clock
clear
74164
74164
14
8
9
1
2
3kΩ
3 - 6
10 - 13
out
common rail


2
3
4
5
6
7
8
9.
10.

+12

IN →

−12V

0V

OUT

Bleu étoilé.
(3-étoiles)